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# Foxconn Precision Co. Inc.

## G31M04 Schematic

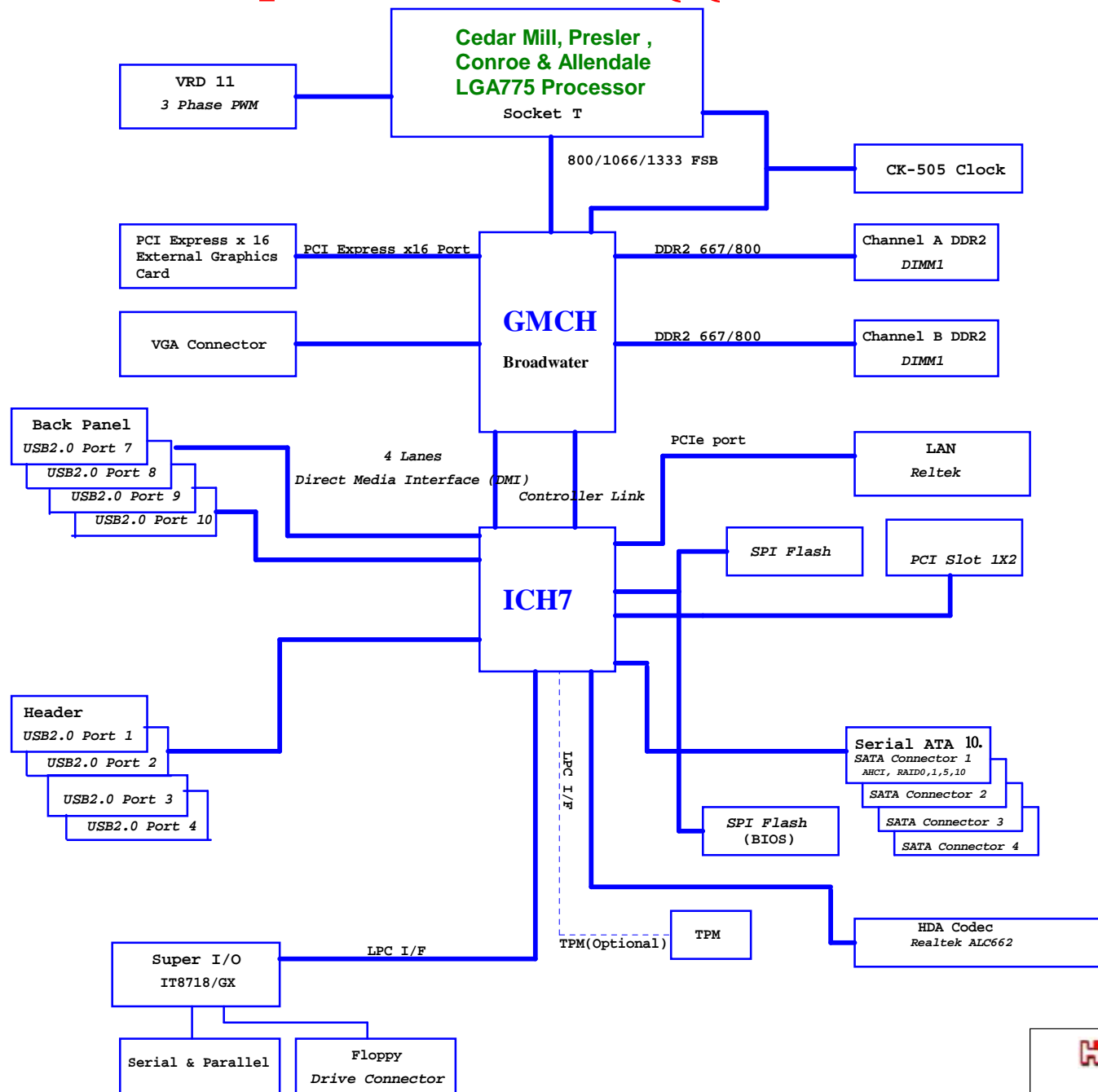
Fab.A  
Data: 2007/6/15

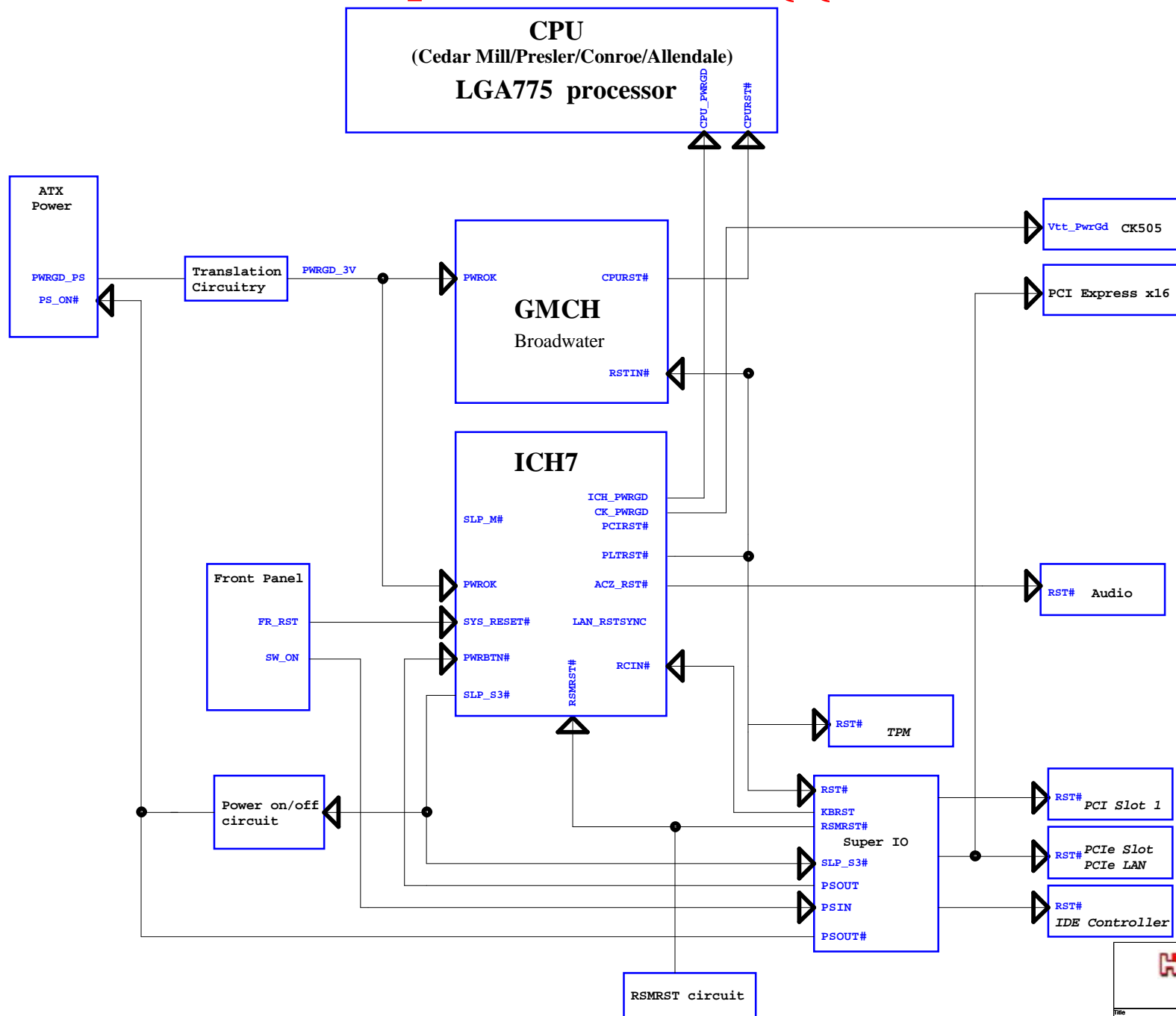
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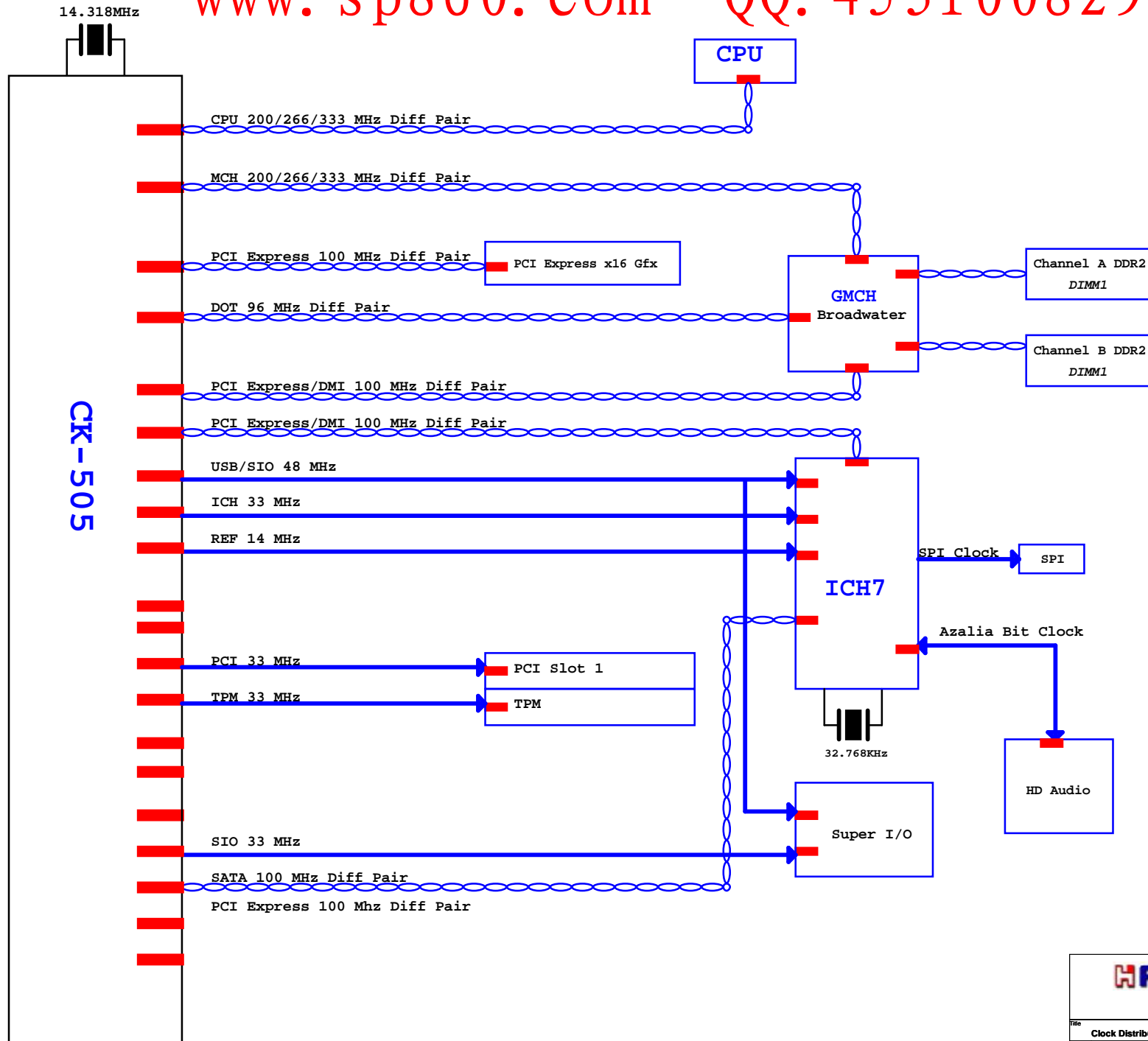
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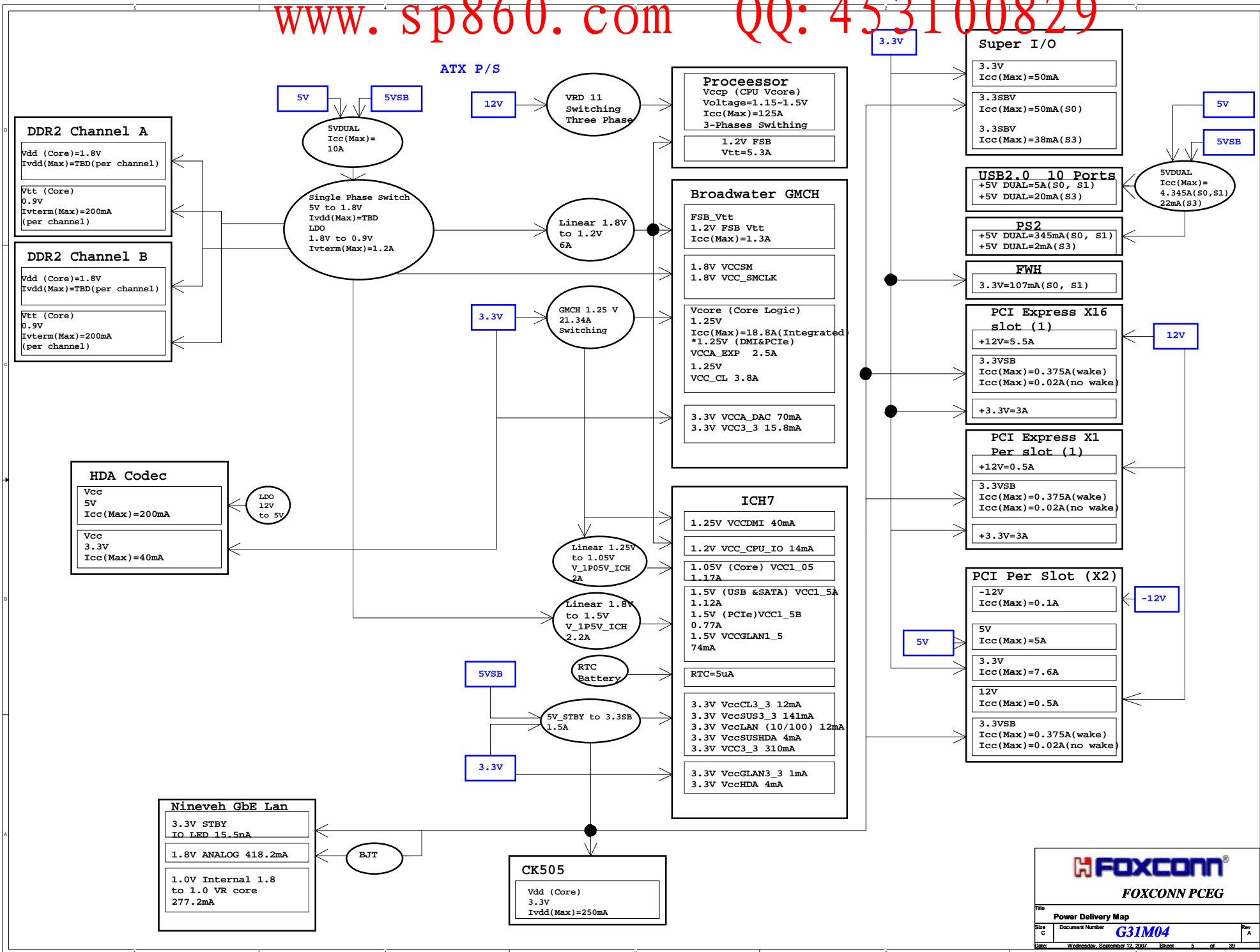


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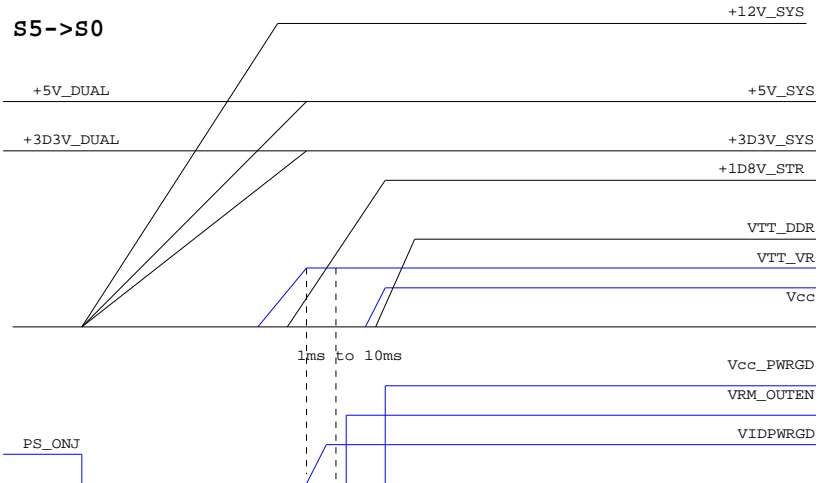




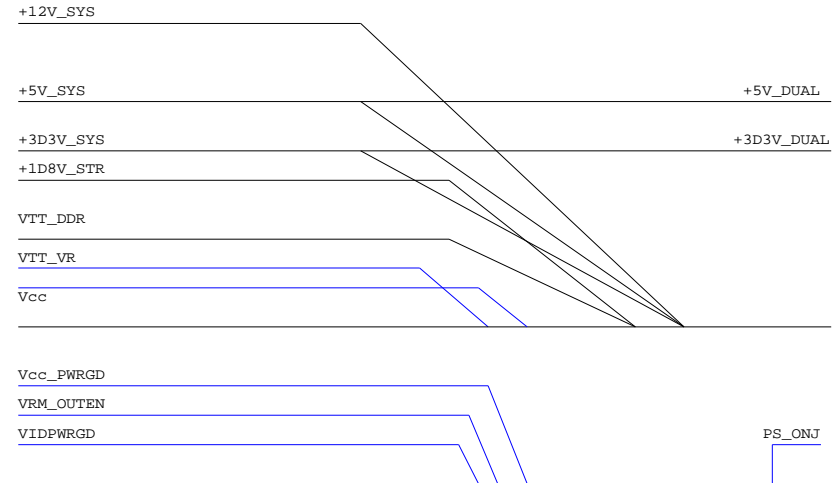




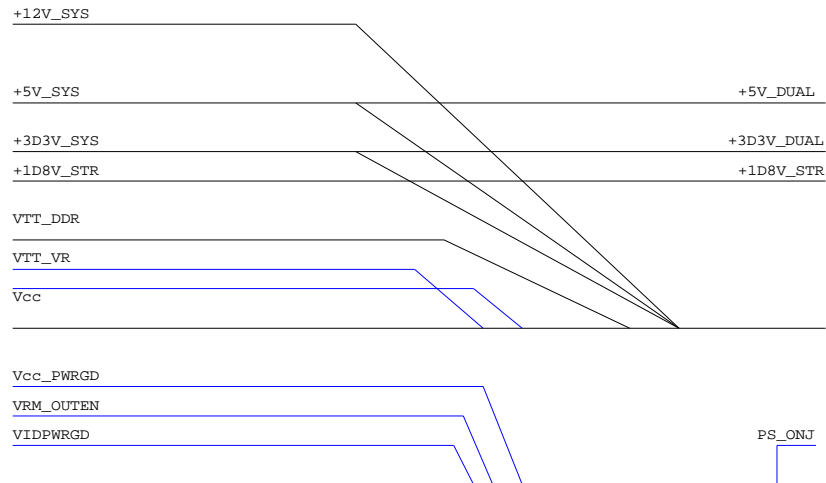
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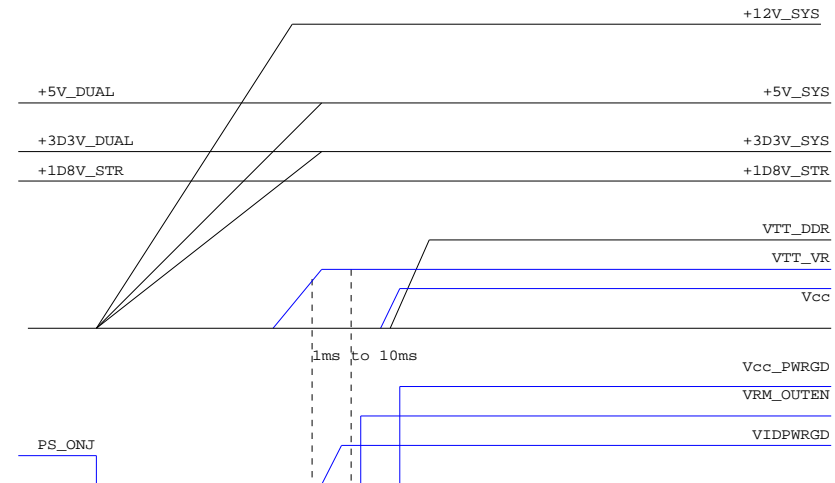
### S0->S5



### S0->S3



### S3->S0



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B  
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D  
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B  
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Title

**BLANK**

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A

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A

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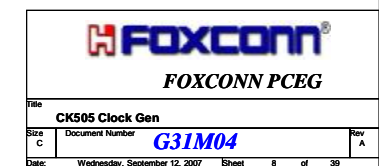
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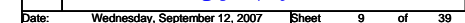
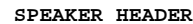
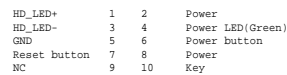
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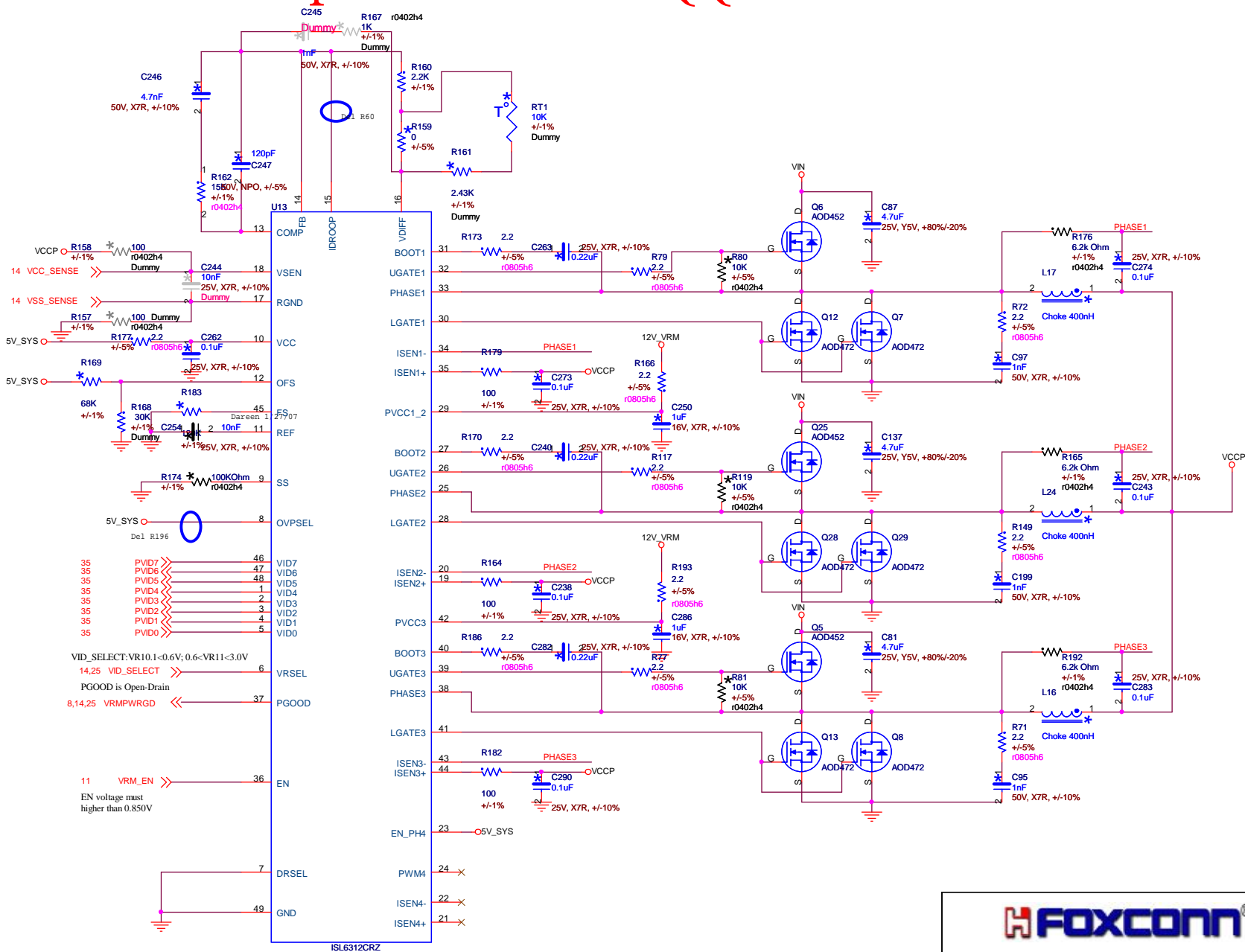
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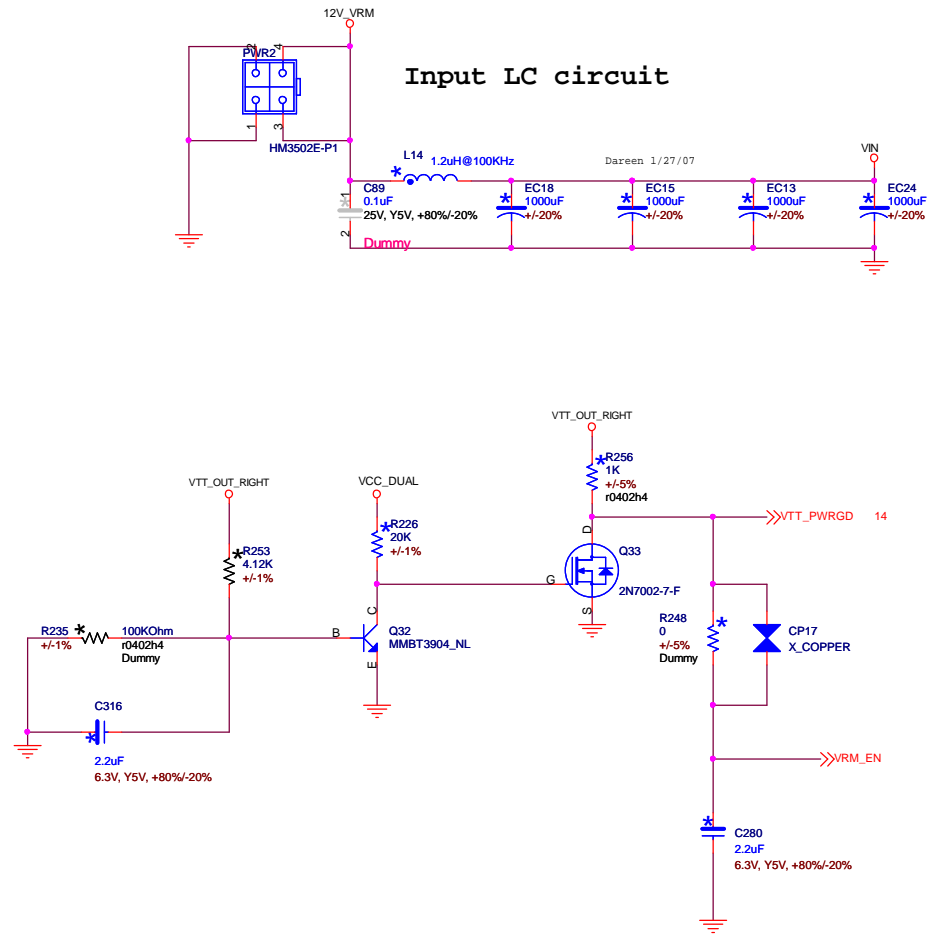
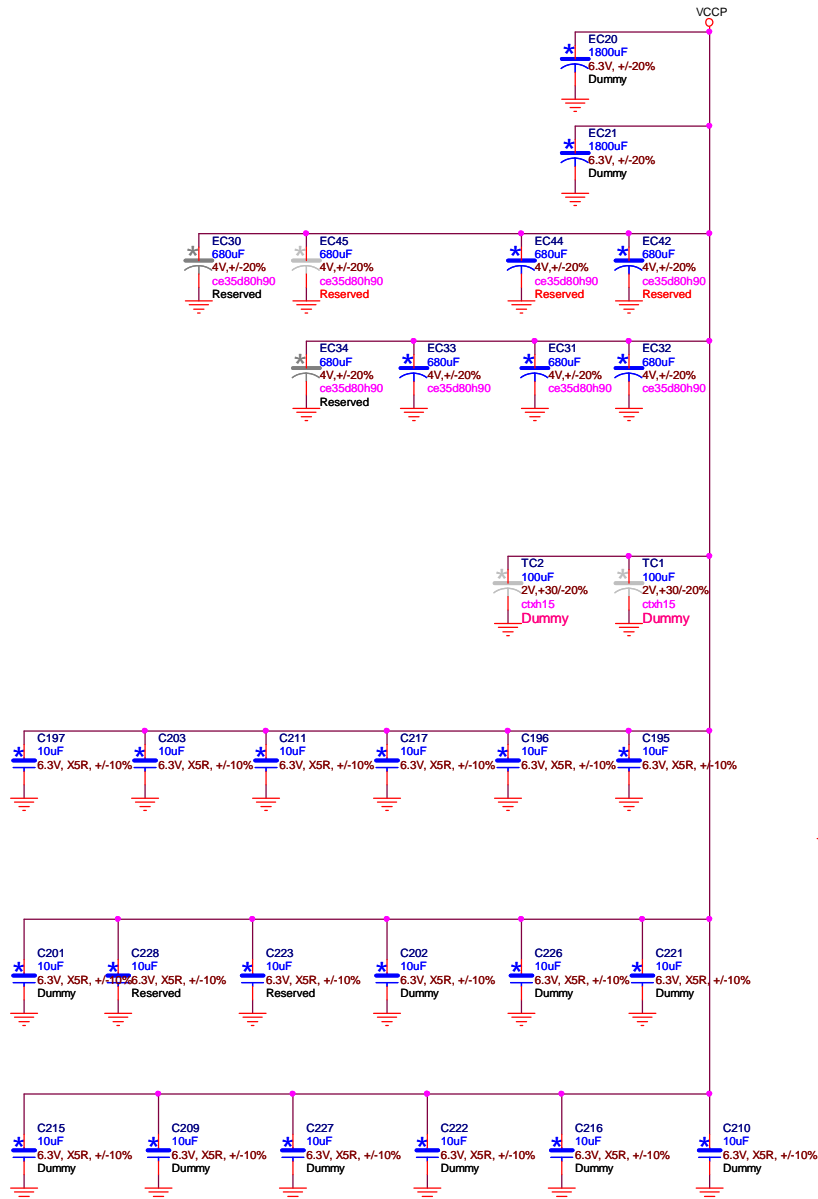


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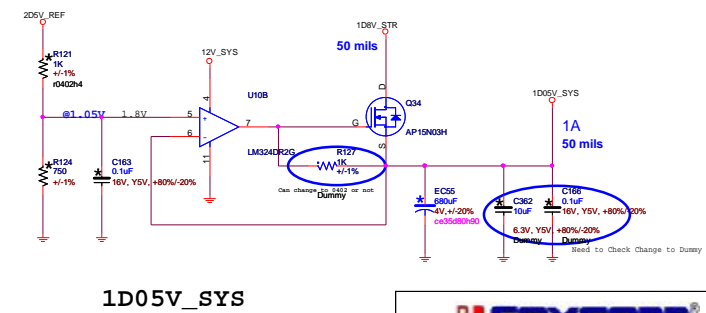
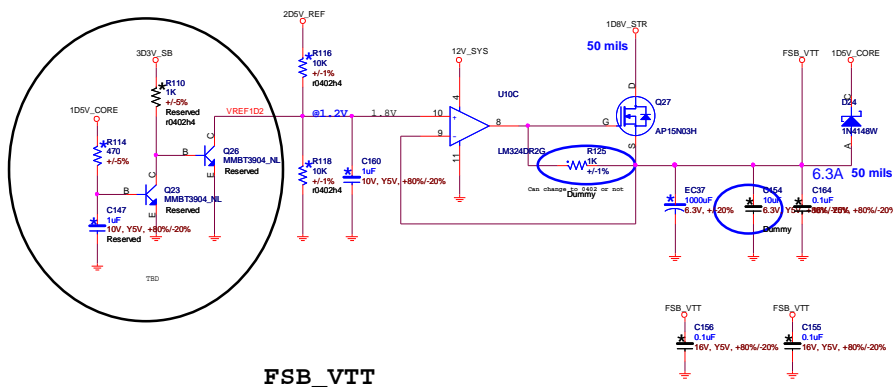
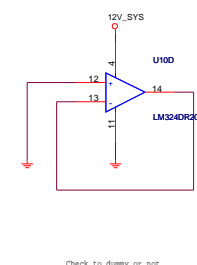
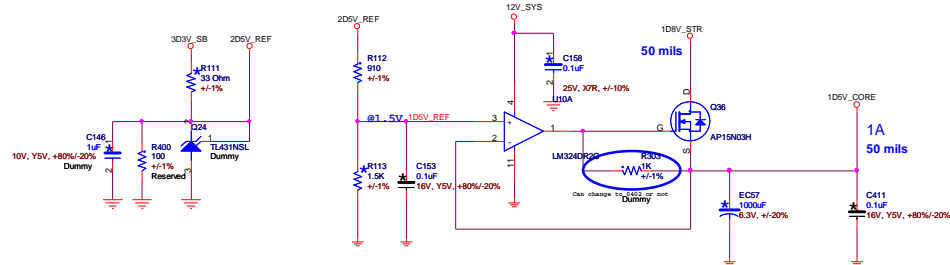
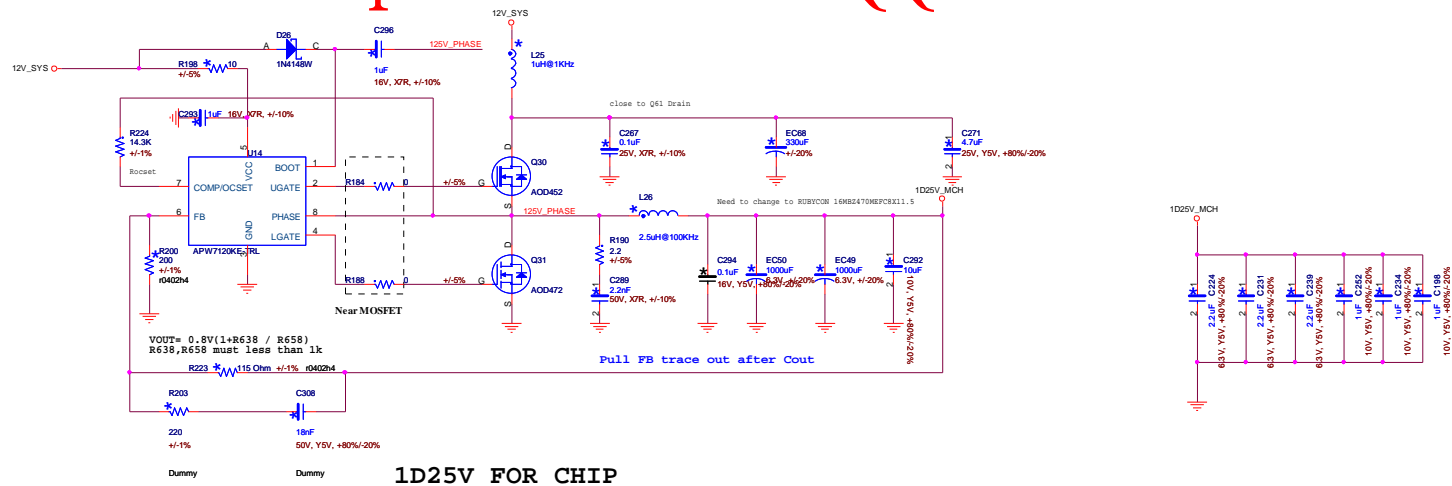
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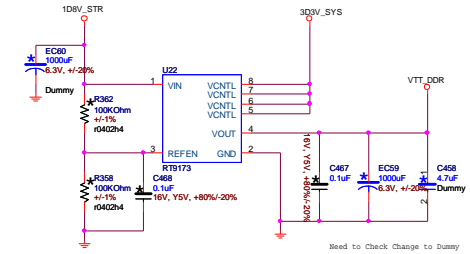
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OUTPUT CAP		
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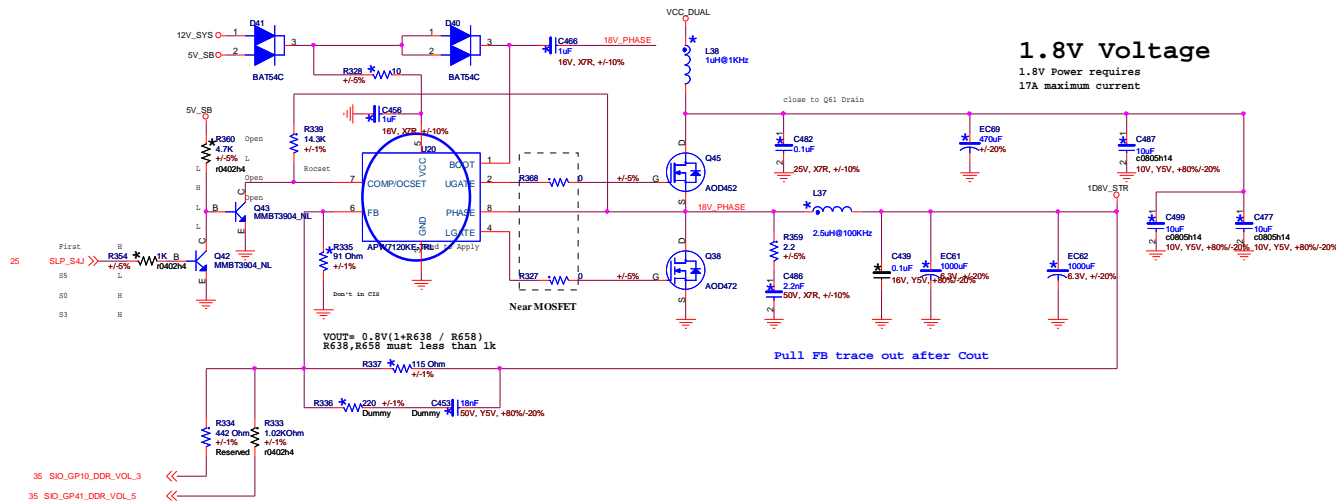
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Title: 1D25V 1D5V FSB	
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## DDR\_VTT

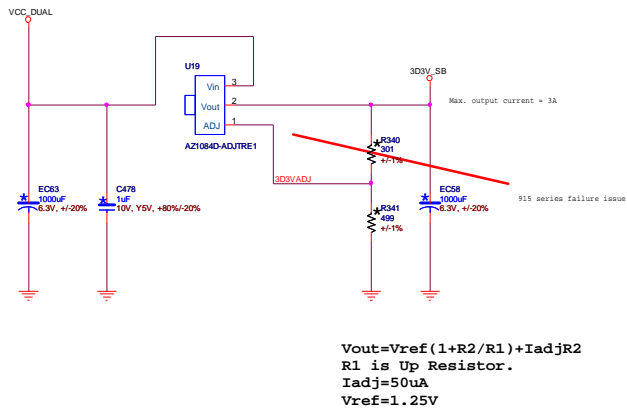


## 1.8V Voltage

1.8V Power requires  
17A maximum current



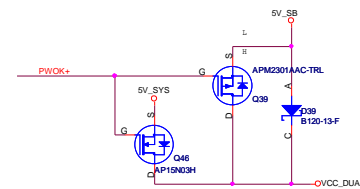
## 1D8V\_STR



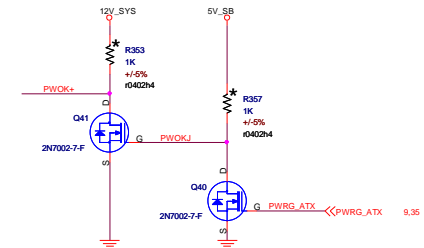
$$V_{out} = V_{ref} \left( 1 + \frac{R_2}{R_1} \right) + I_{adj} R_2$$

R1 is Up Resistor.  
Iadj=50uA  
Vref=1.25V

## 3D3V\_DUAL



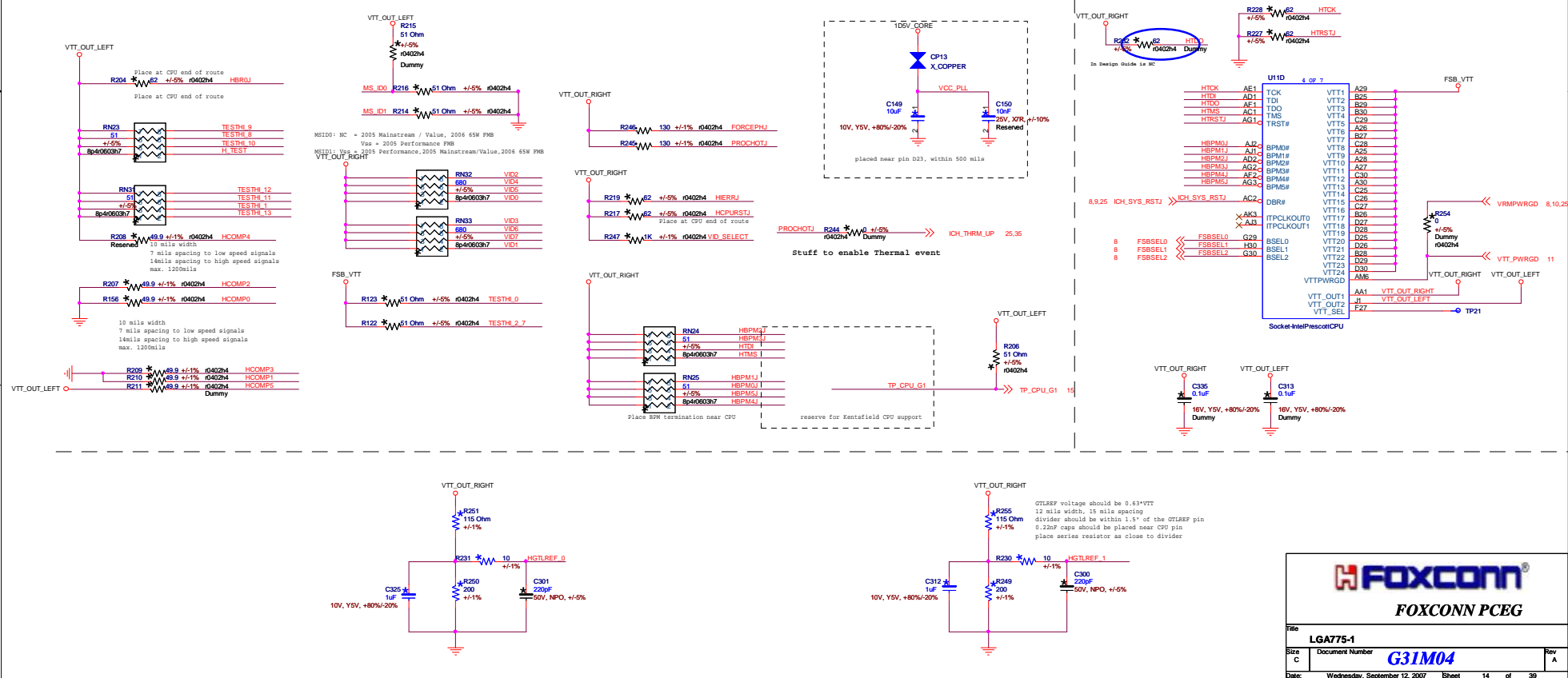
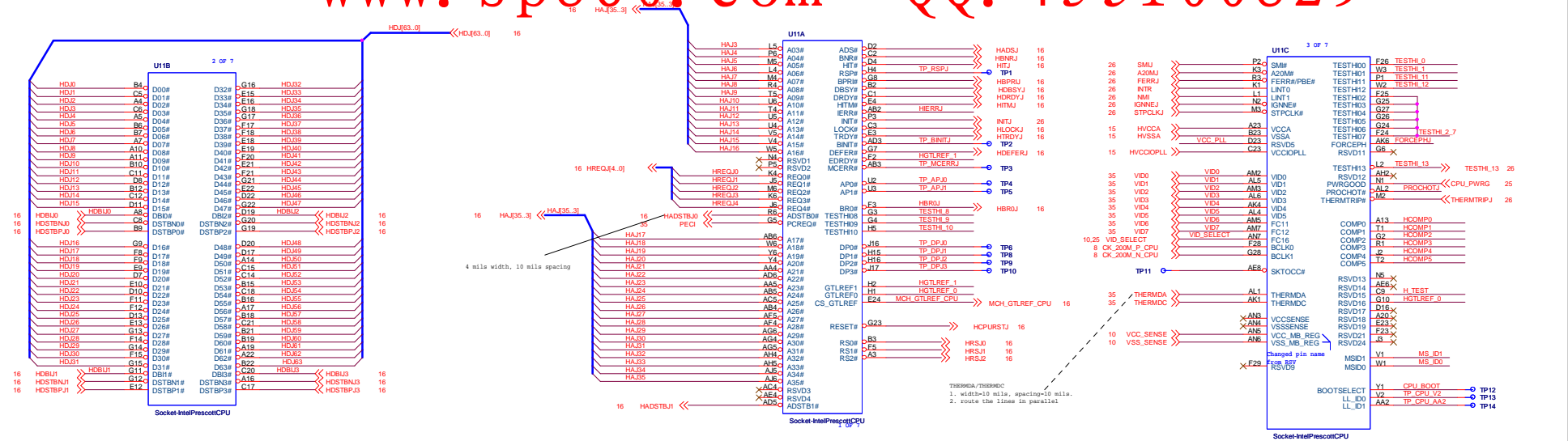
## 5V\_DUAL

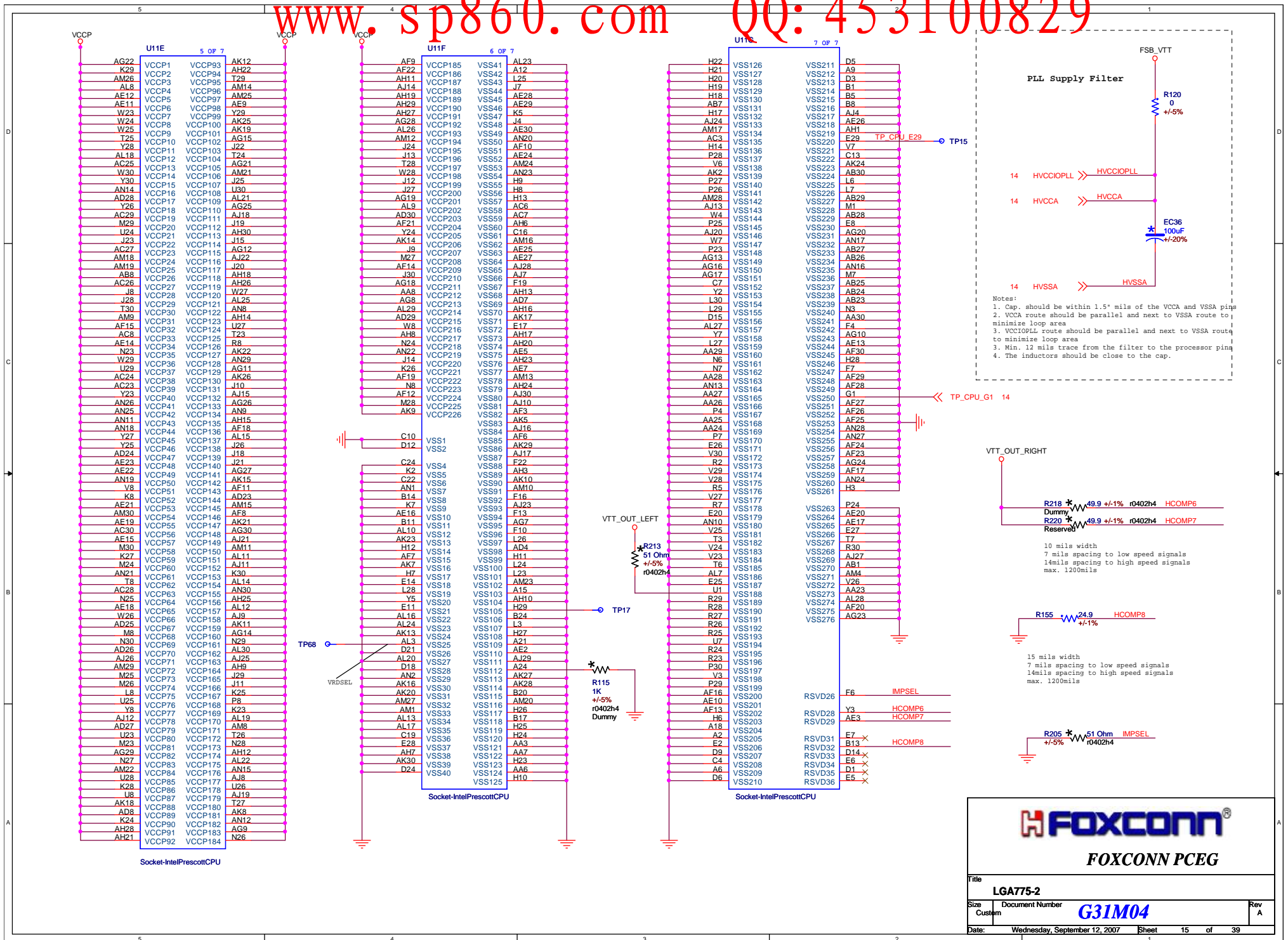


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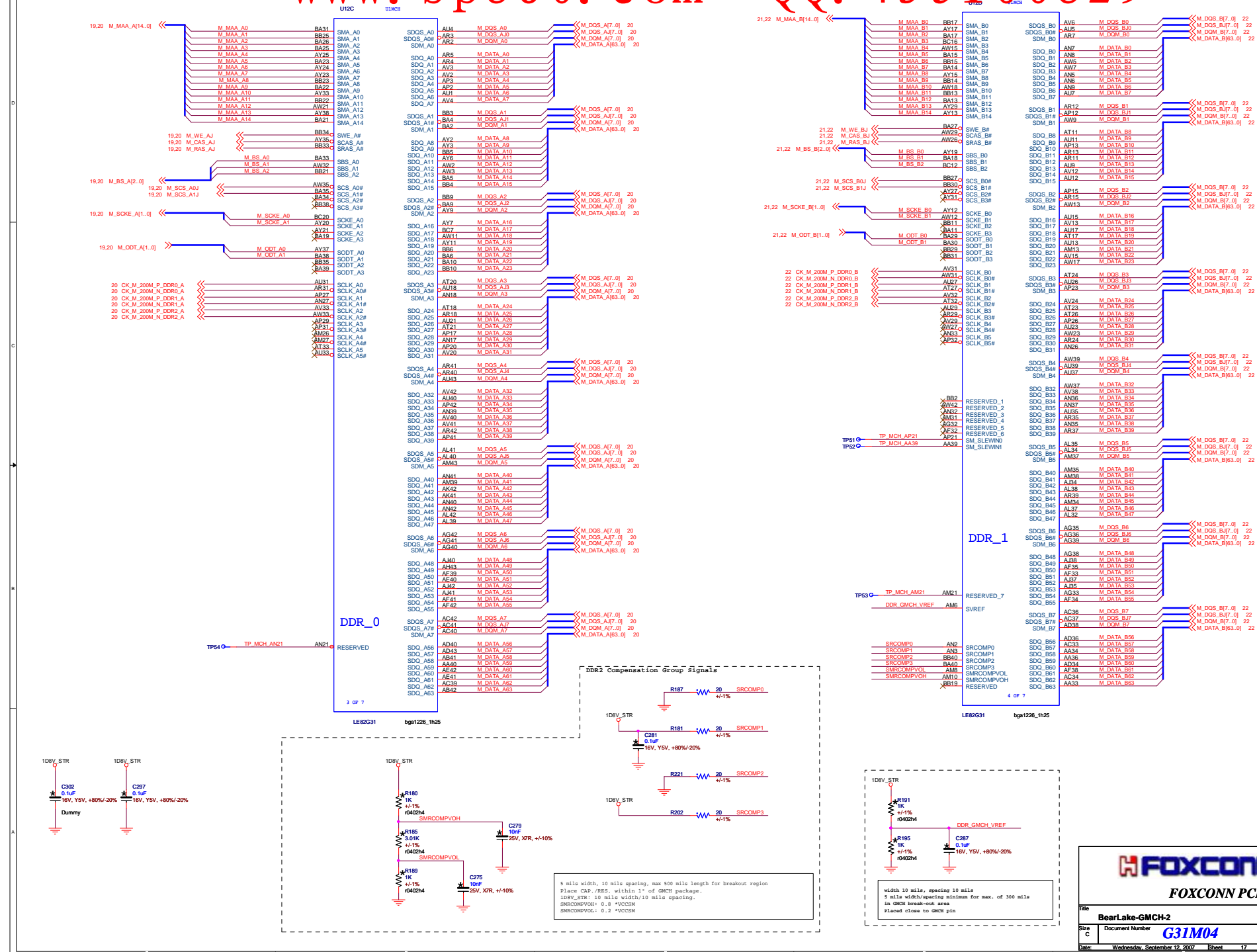


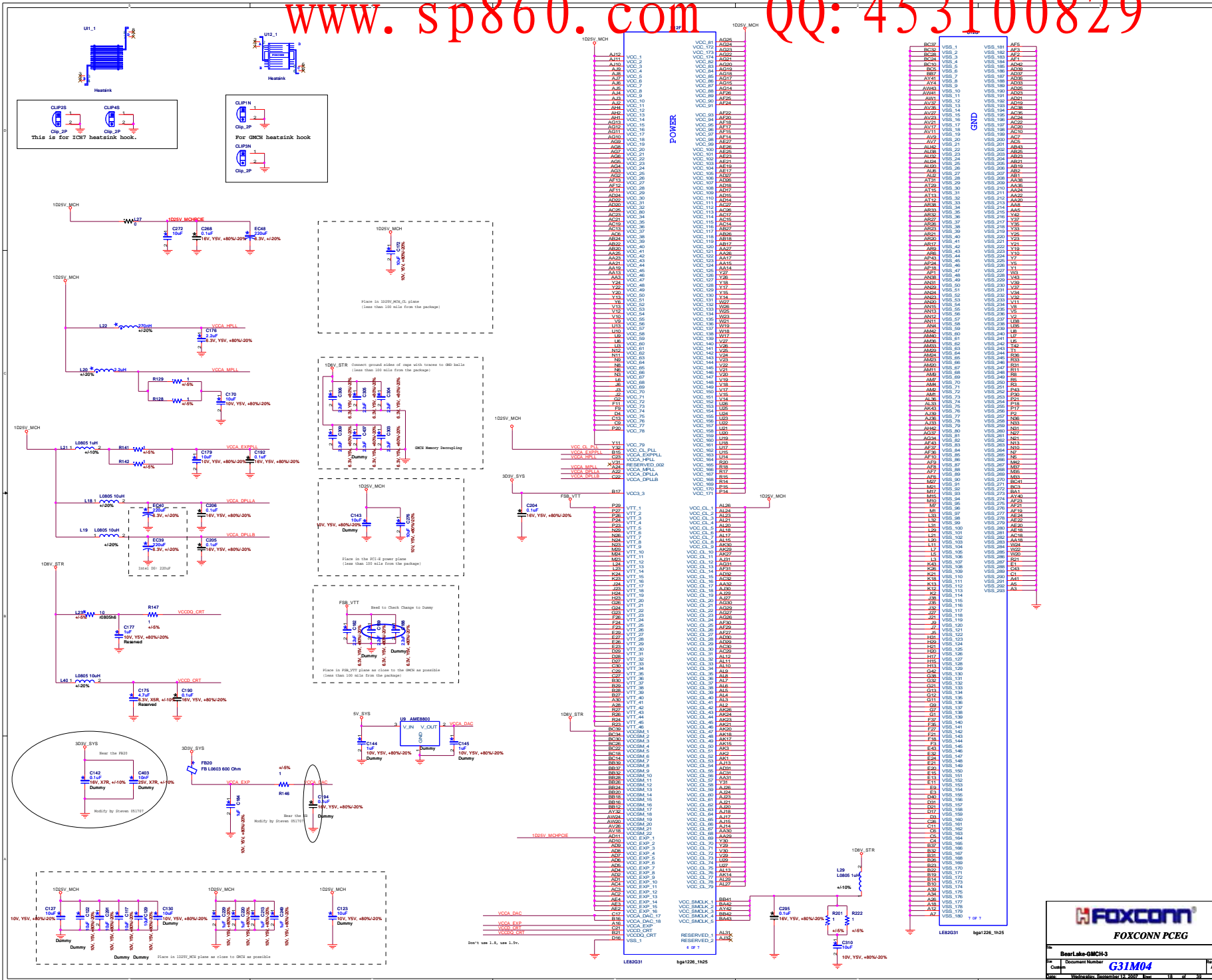


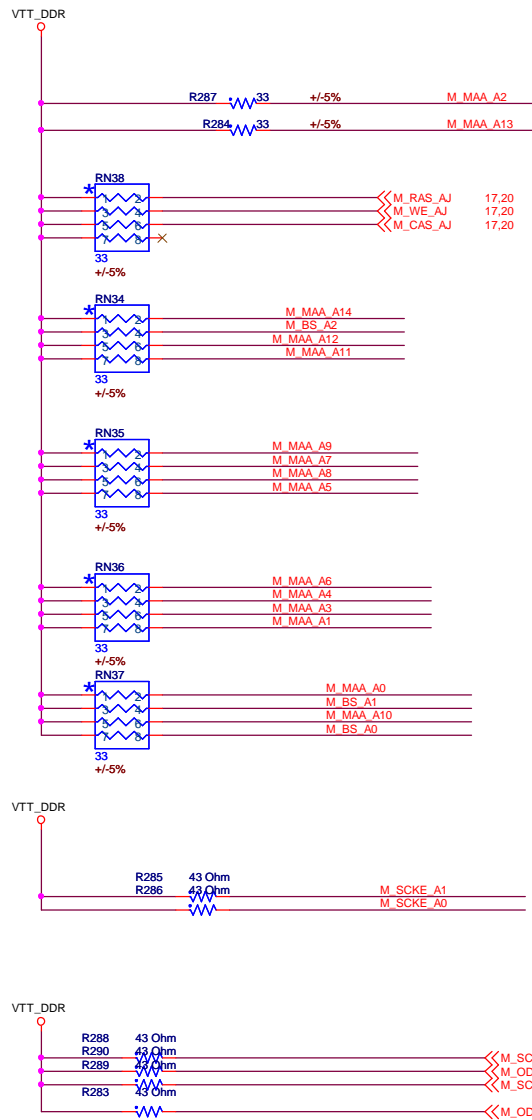




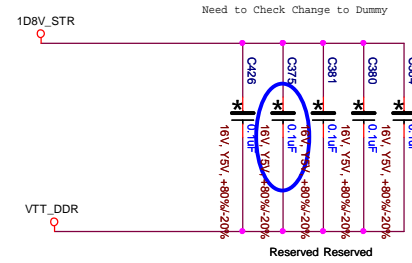
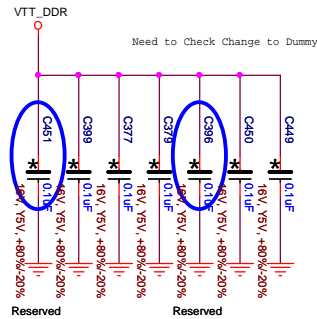




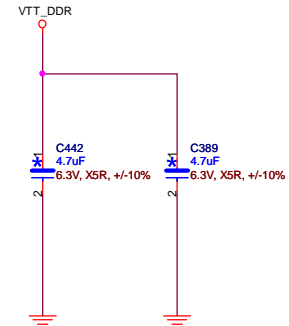




$\ll$  M.ODT\_A[1..0] 17,20  
 $\ll$  M.SCKE\_A[1..0] 17,20  
 $\ll$  M.BS\_A[2..0] 17,20  
 $\ll$  M.MAA\_A[14..0] 17,20



Channel A VTT\_0.9V high-frequency decoupling caps.  
Place as close to termination resistors as possible

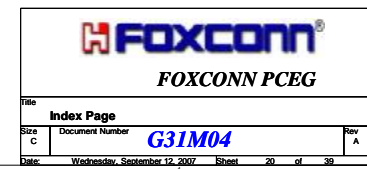


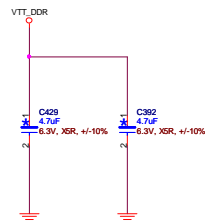
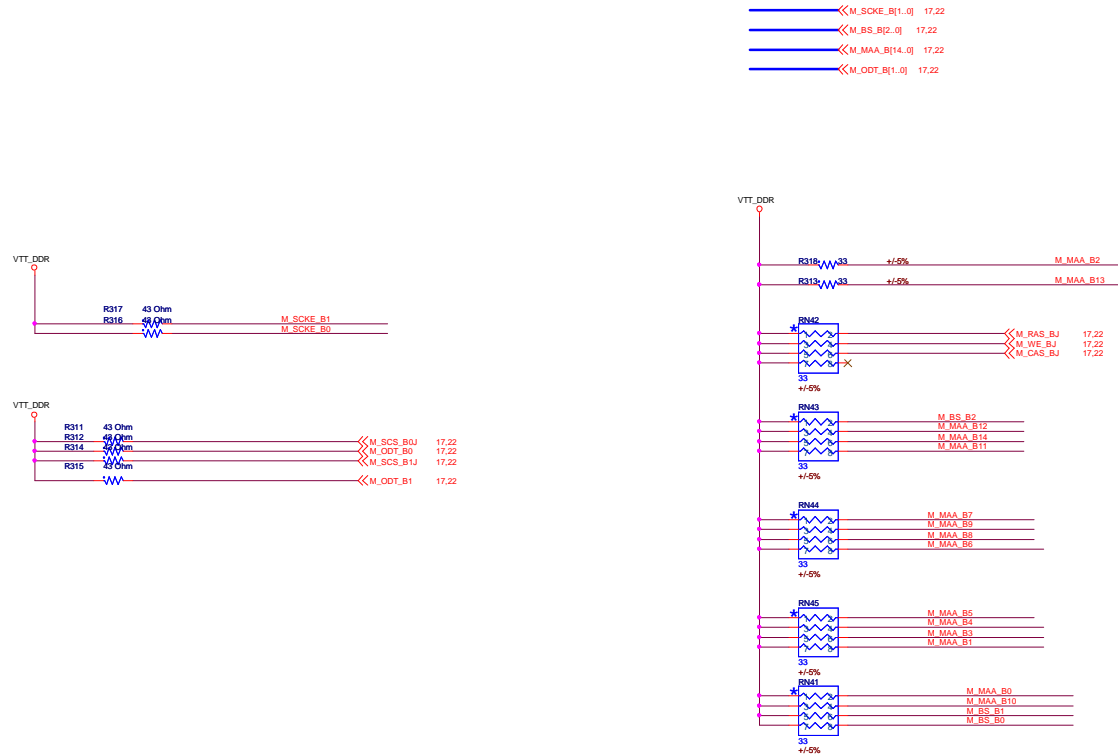
Channel A VTT\_0.9V Mid Range decoupling caps.  
Placed in termination Island



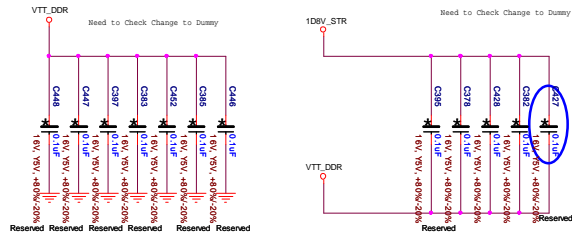
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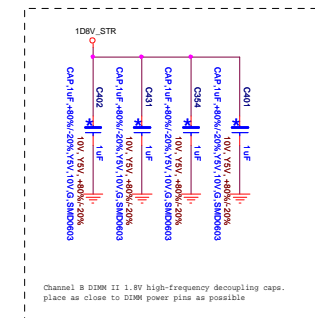
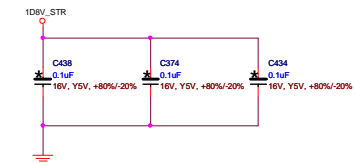
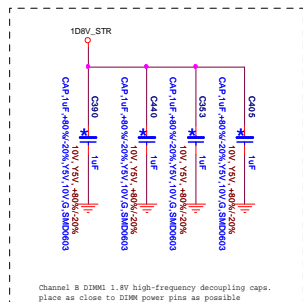


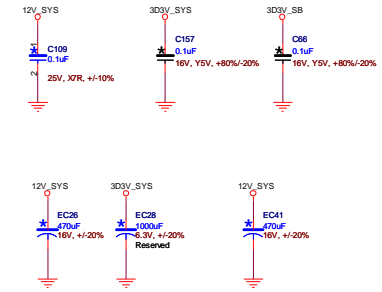
Channel B VTT\_0.9V Mid Range decoupling caps.  
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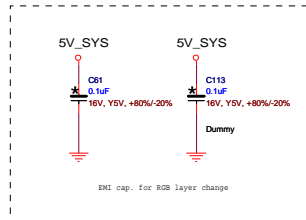


Channel B VTT\_0.9V high-frequency decoupling caps.  
Place as close to termination resistors as possible

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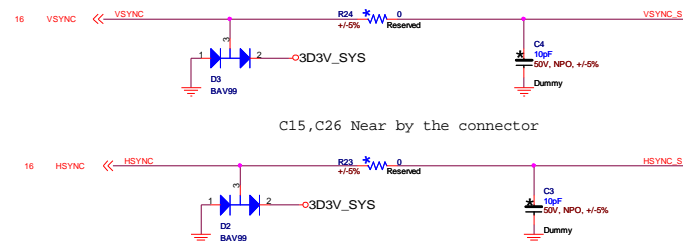
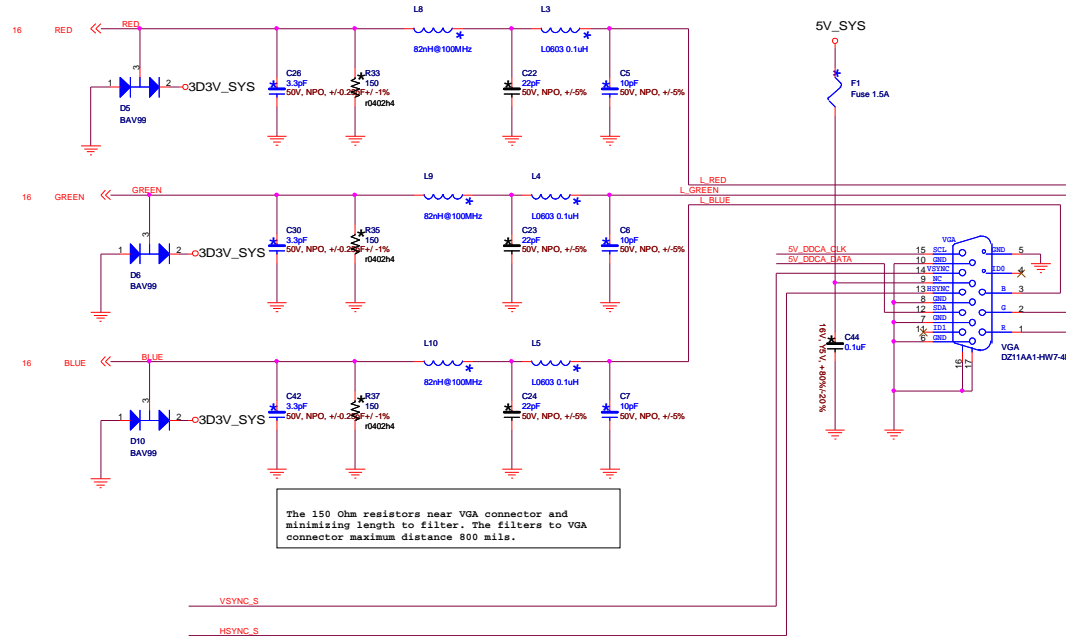
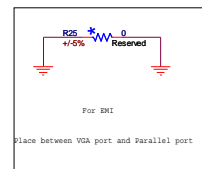
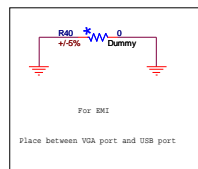
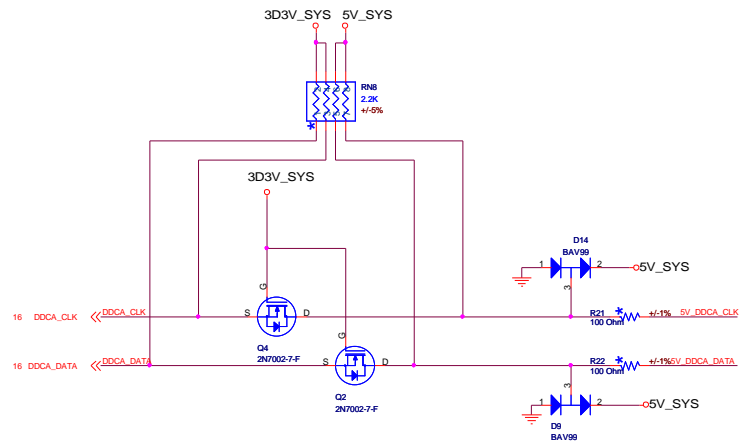






#### RGB routing

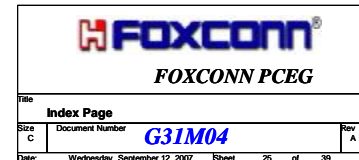
1. from GMCH to the first 150 ohm resistor: 7.5 mils(min. 6 mils spacing )
2. from the first 150 ohm res. to the second 150 ohm resistor: 4 mils
3. from the second 150 ohm resistor to connector: 4 mils
4. spacing minimum 6 mils, 30 mils spacing is recommended
5. R,G,B should be length matched to 700 mils, max. length is 8400 mils
6. R,G,B signals should be ground referenced

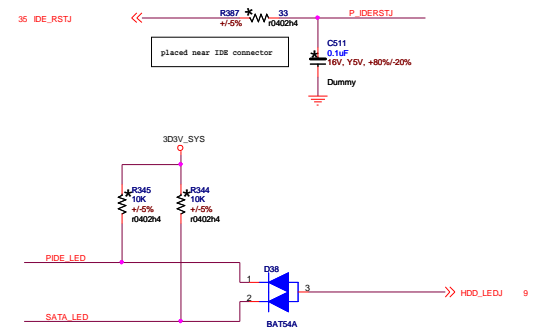
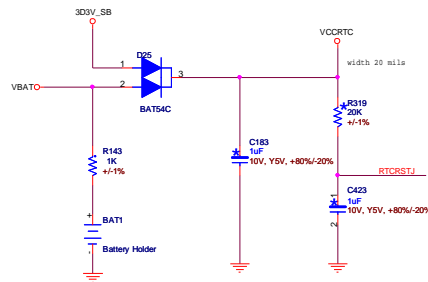
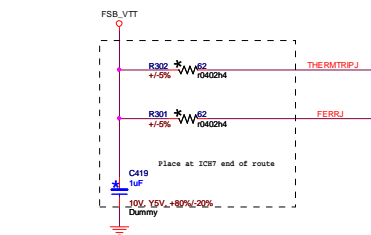
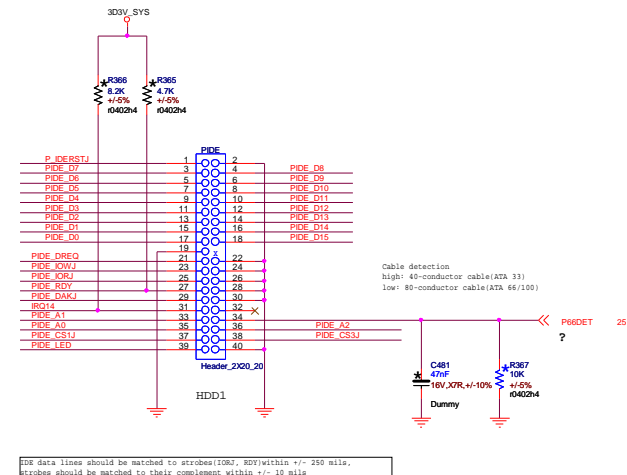
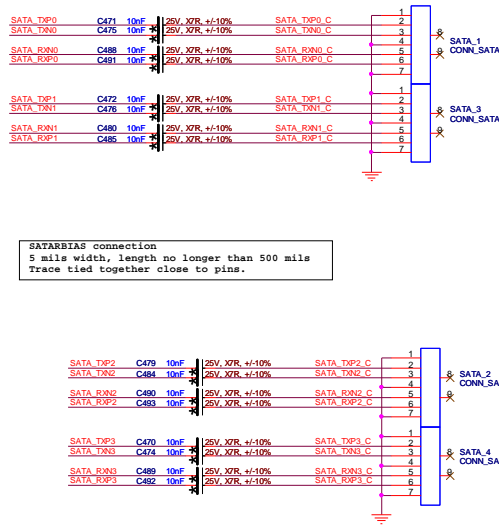
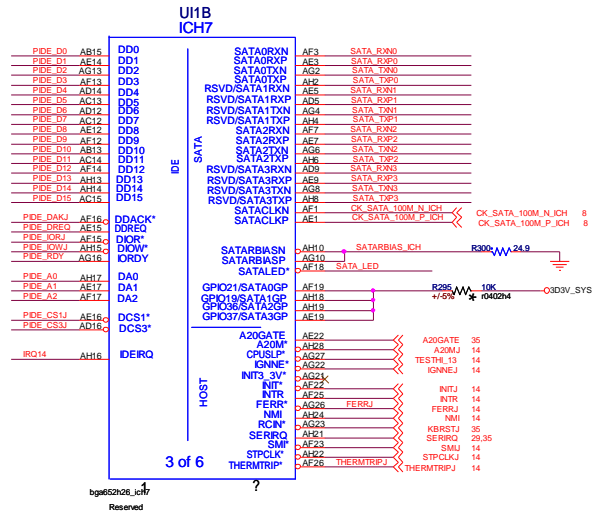


C15,C26 Near by the connector

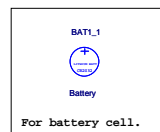
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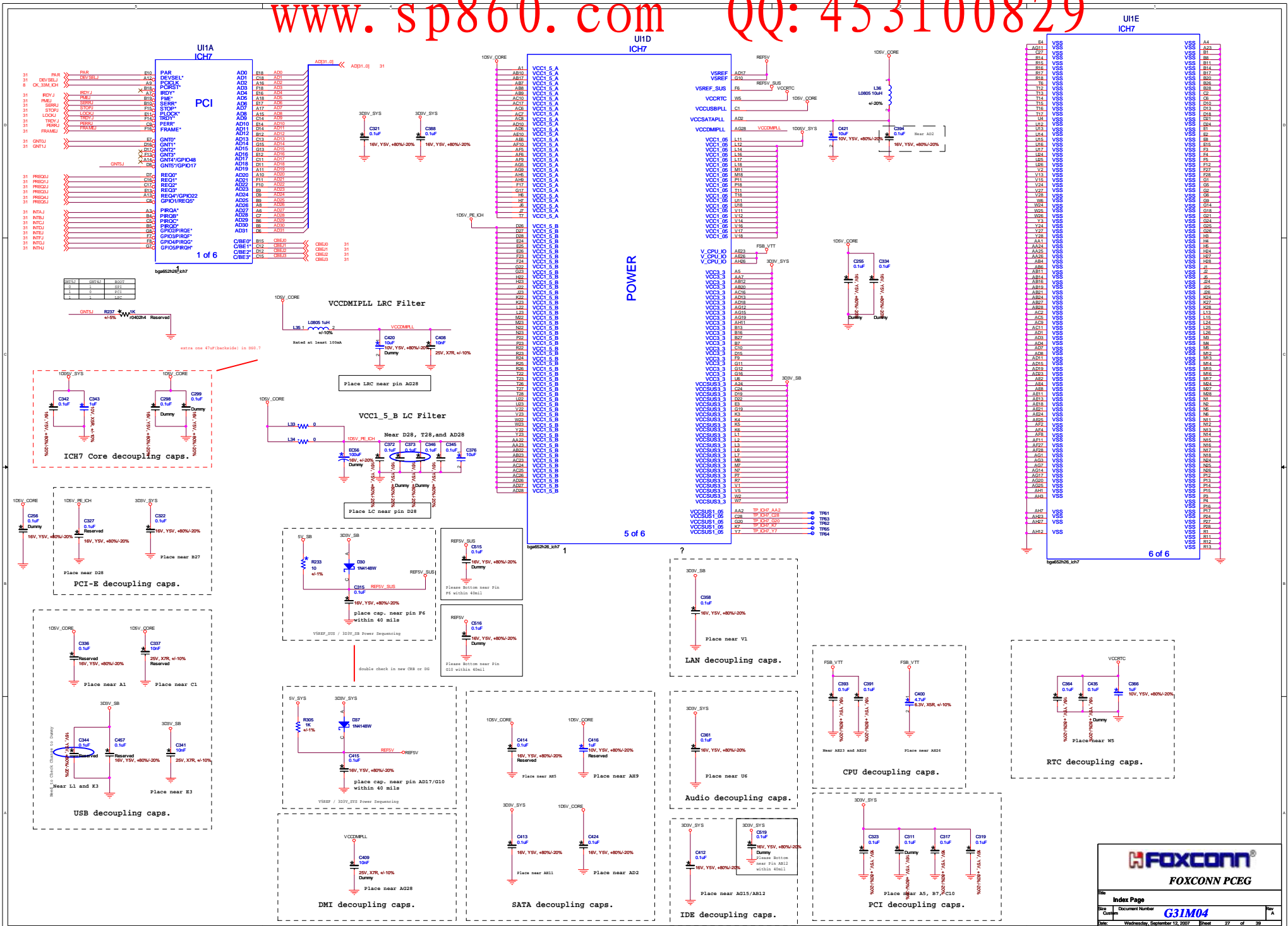




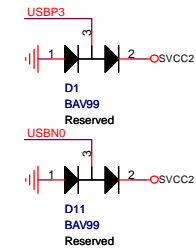
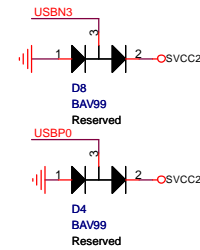
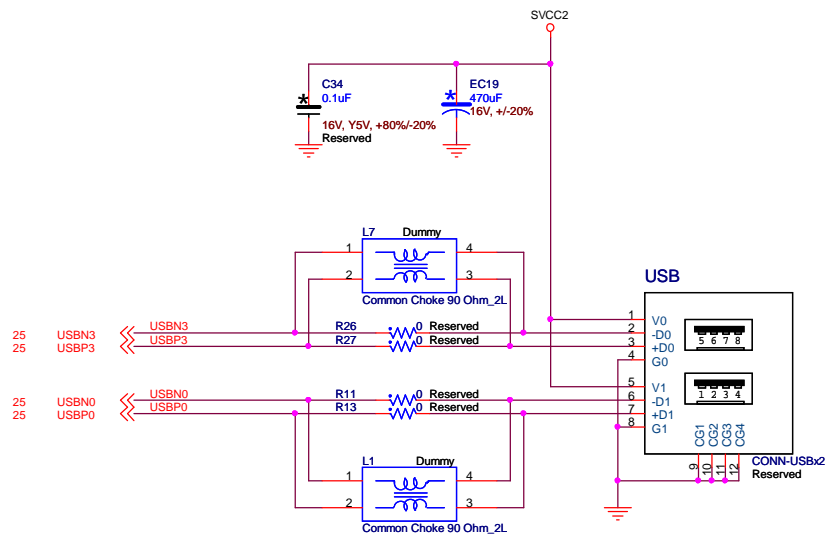


CLR_CMOS	CMOS
Clear	(1-2)
Normal	(2-3) <b>Default</b>





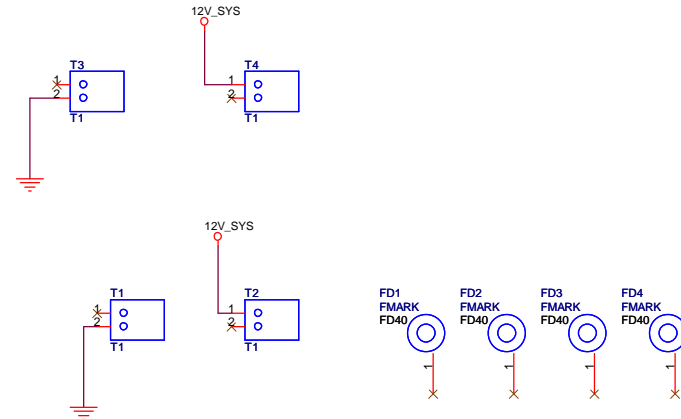
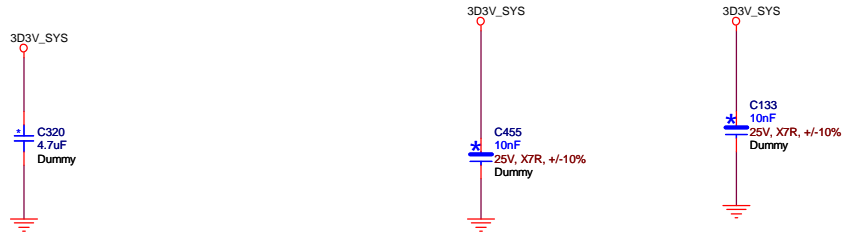
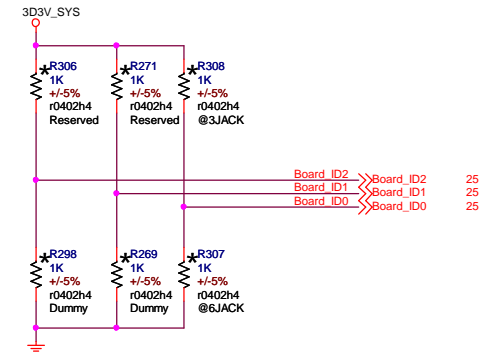
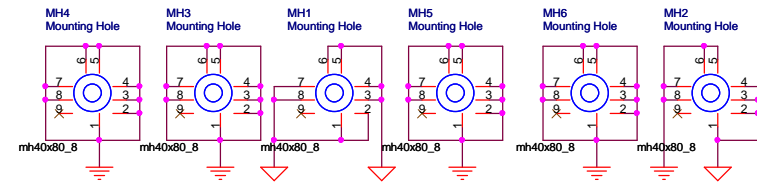
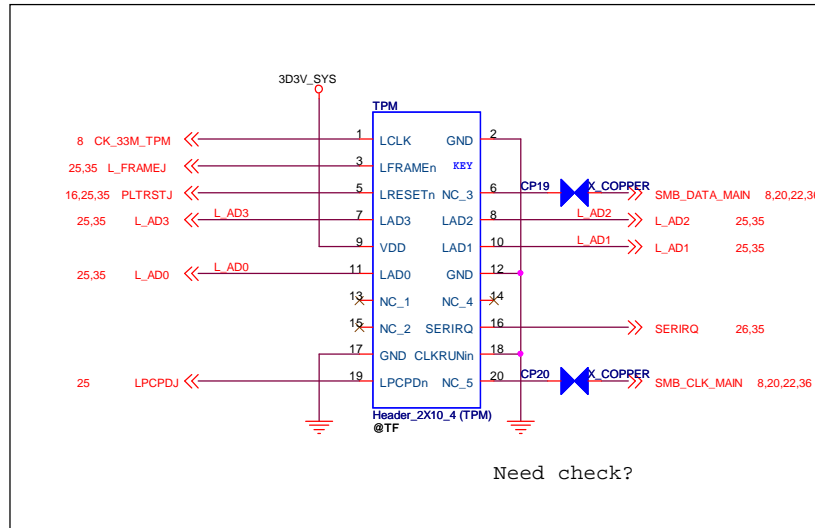
## Rear Dual USB Connector



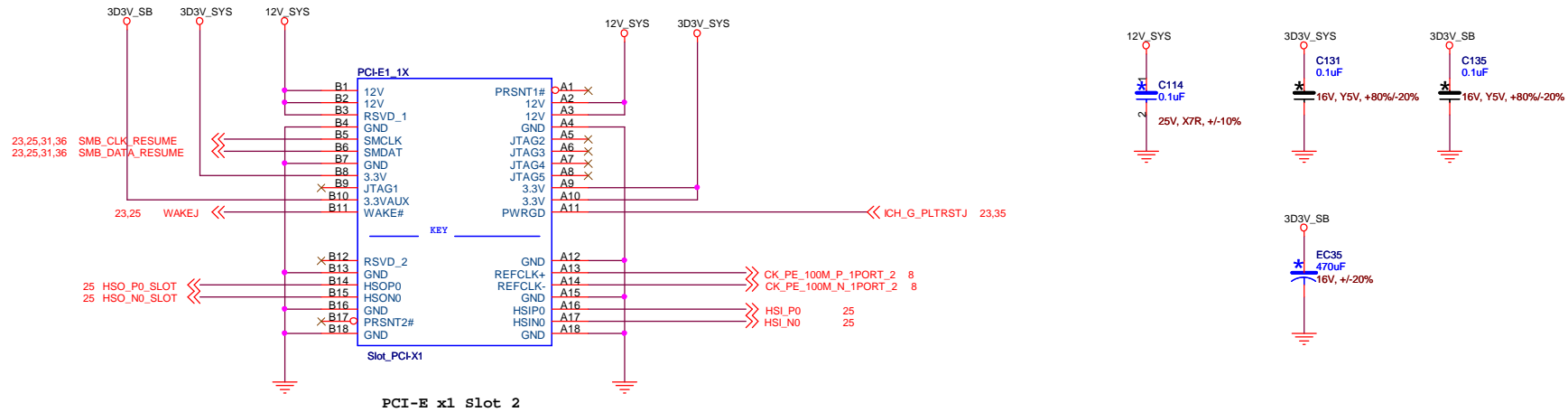
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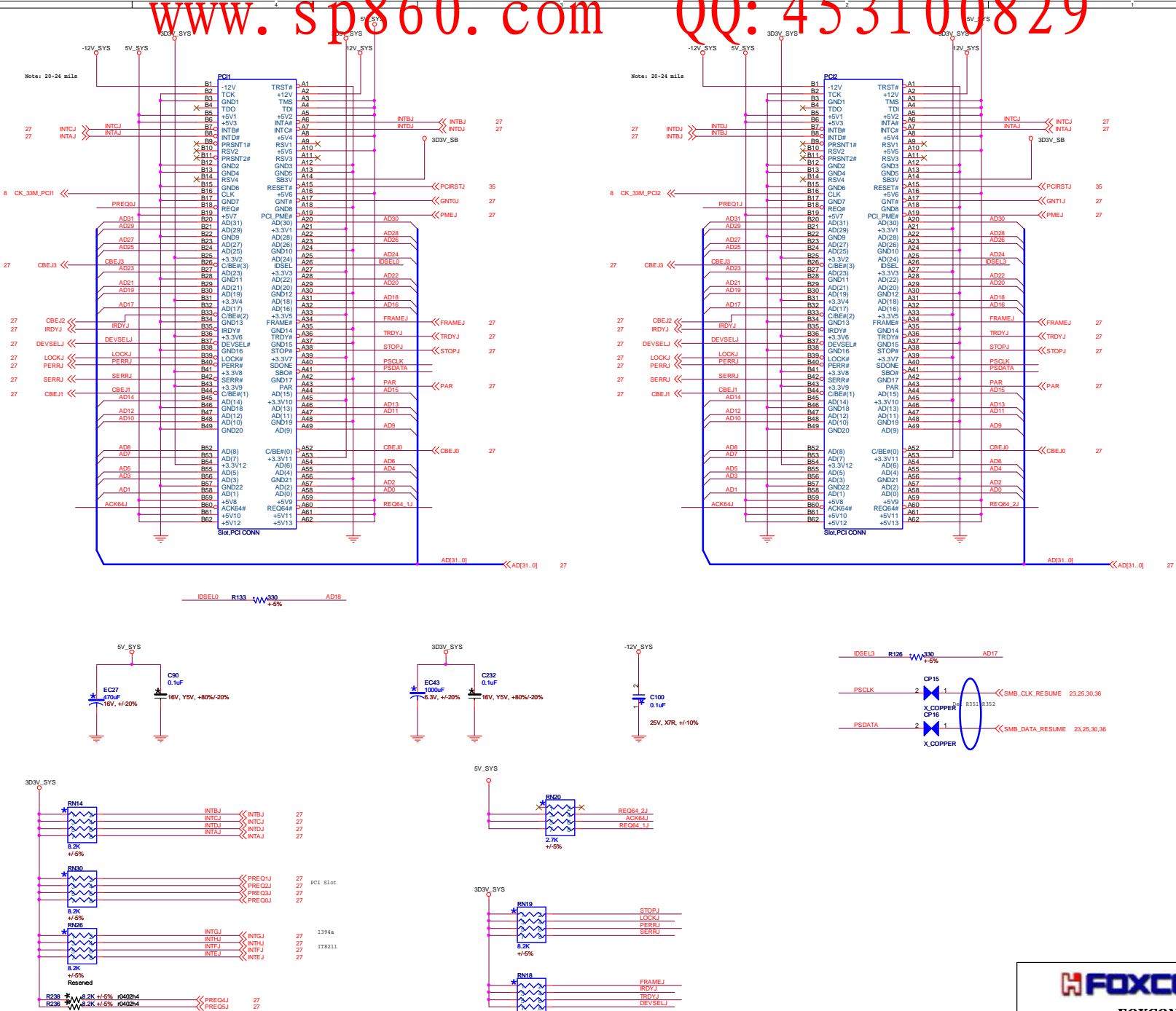
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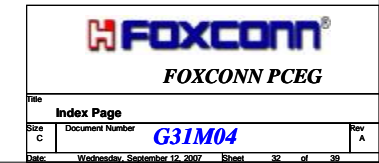


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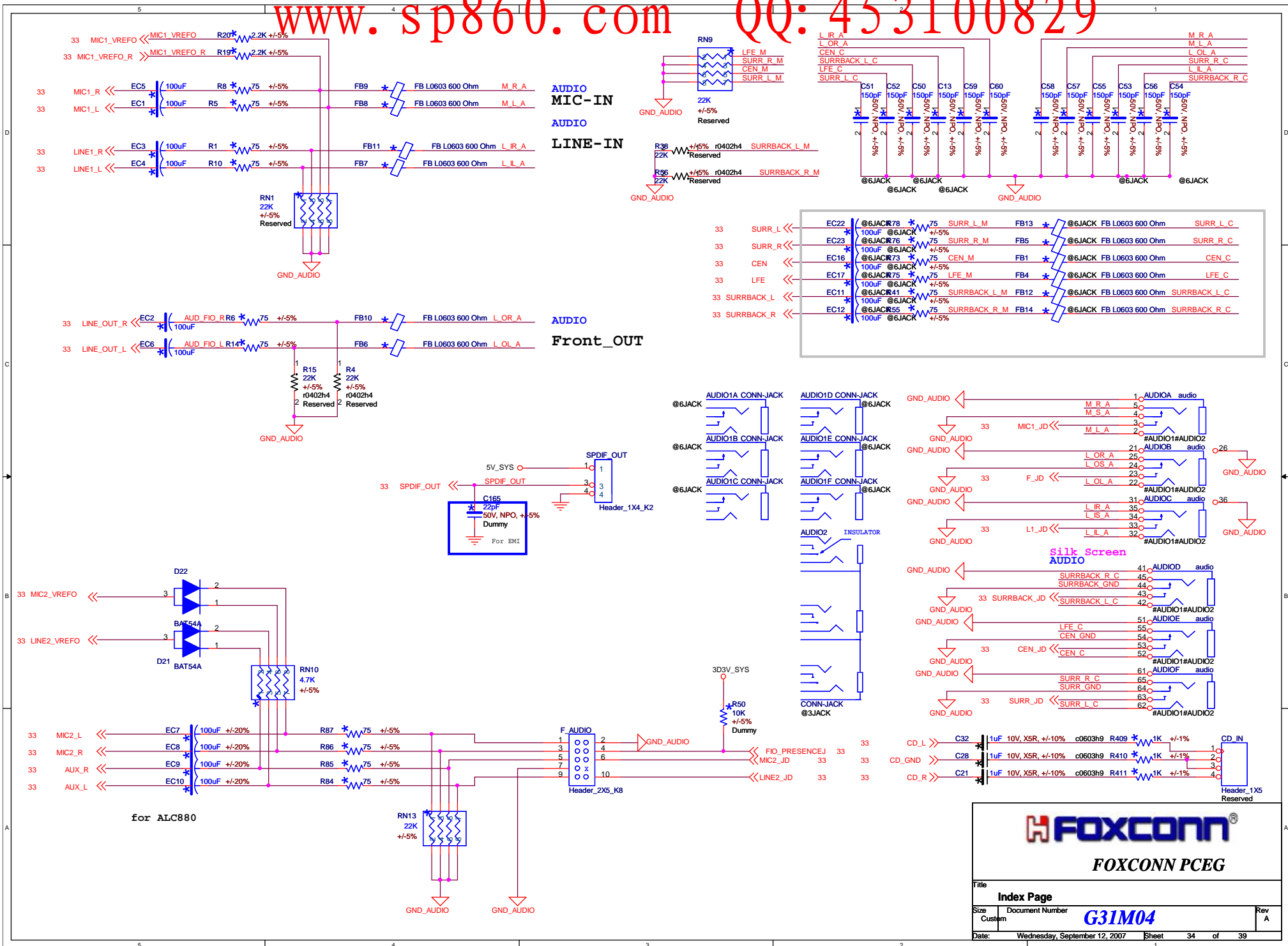


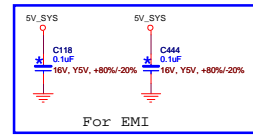
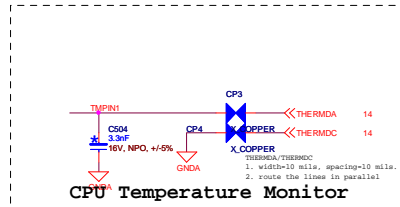
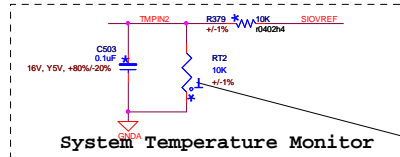
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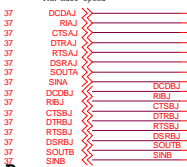




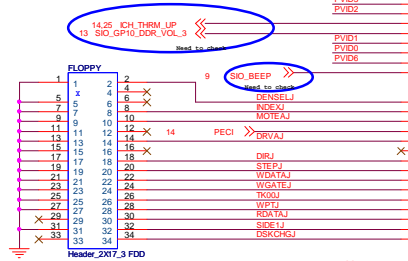




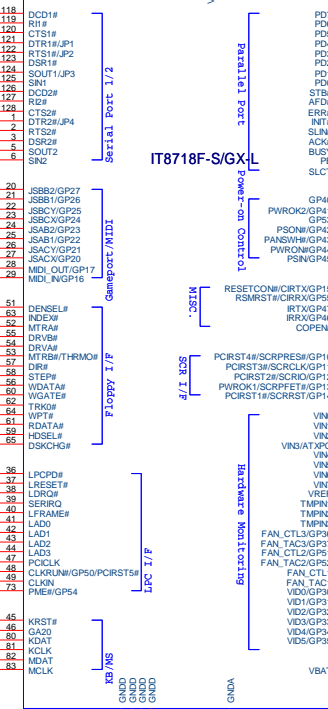
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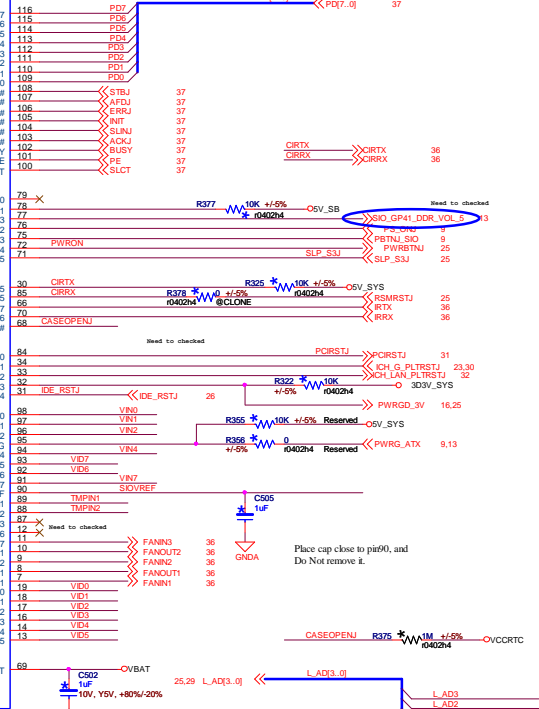
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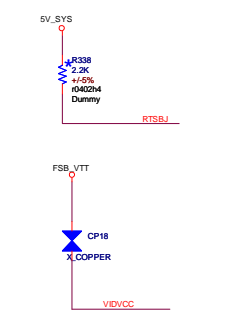
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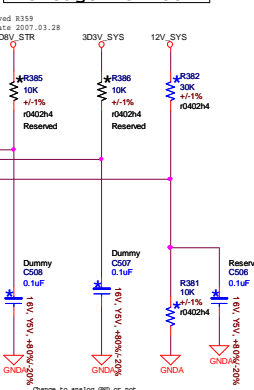
#### Printer



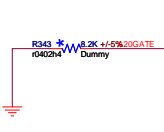
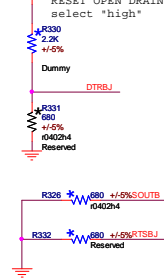
Update by ITE Gary 0202



#### Voltage Monitor

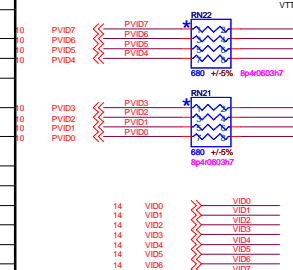


#### RESET OPEN DRAIN



#### Power On Strapping Options

Symbol	value	Description
JP1 Pin 121	FlashSeg1_EN	0 Disabled. 1 Flash IF Address Segment 1 (FFFF_0000h-FFFF_FFFFh, 000F_0000h-000F_FFFFh) is enabled
JP2 Pin 122	VIDO_EN	0 Disable VID output pins 1 Enable VID output pins
JP3 Pin 124	CHIP_SEL	0 Use for chip 1 when two IT8718F exit in the same system. Chip is selected in conjunction with "Global Configuration Register - Index 22, bit 7" 1 Use for chip 0 when two IT8718F exit in the same system. Chip is selected in conjunction with "Global Configuration Register - Index 22, bit 7"
JP4 Pin 1	BUF_SEL	0 The output buffers of PCIRST1#, PCIRST2#, PCIRST3# and PCIRST4# are open-drain. 1 The output buffers are push-pull.
JP5:JP7 Pin 2 & 46	FAN_CTL_SEL	11 The default value of EC Index 15h / 16h / 17h is 00h 10 The default value of EC Index 15h / 16h / 17h is 20h 01 The default value of EC Index 15h / 16h / 17h is 40h 00 The default value of EC Index 15h / 16h / 17h is 60h
JP6 Pin 5	VID_ISEL	1 The threshold voltage of VID is 2.0 / 0.8V 0 The threshold voltage of VID is 0.8 / 0.4V
JP7 Pin 46	WDT_EN	1 Disable WDT to reset PWROK 0 Enable WDT to reset PWROK

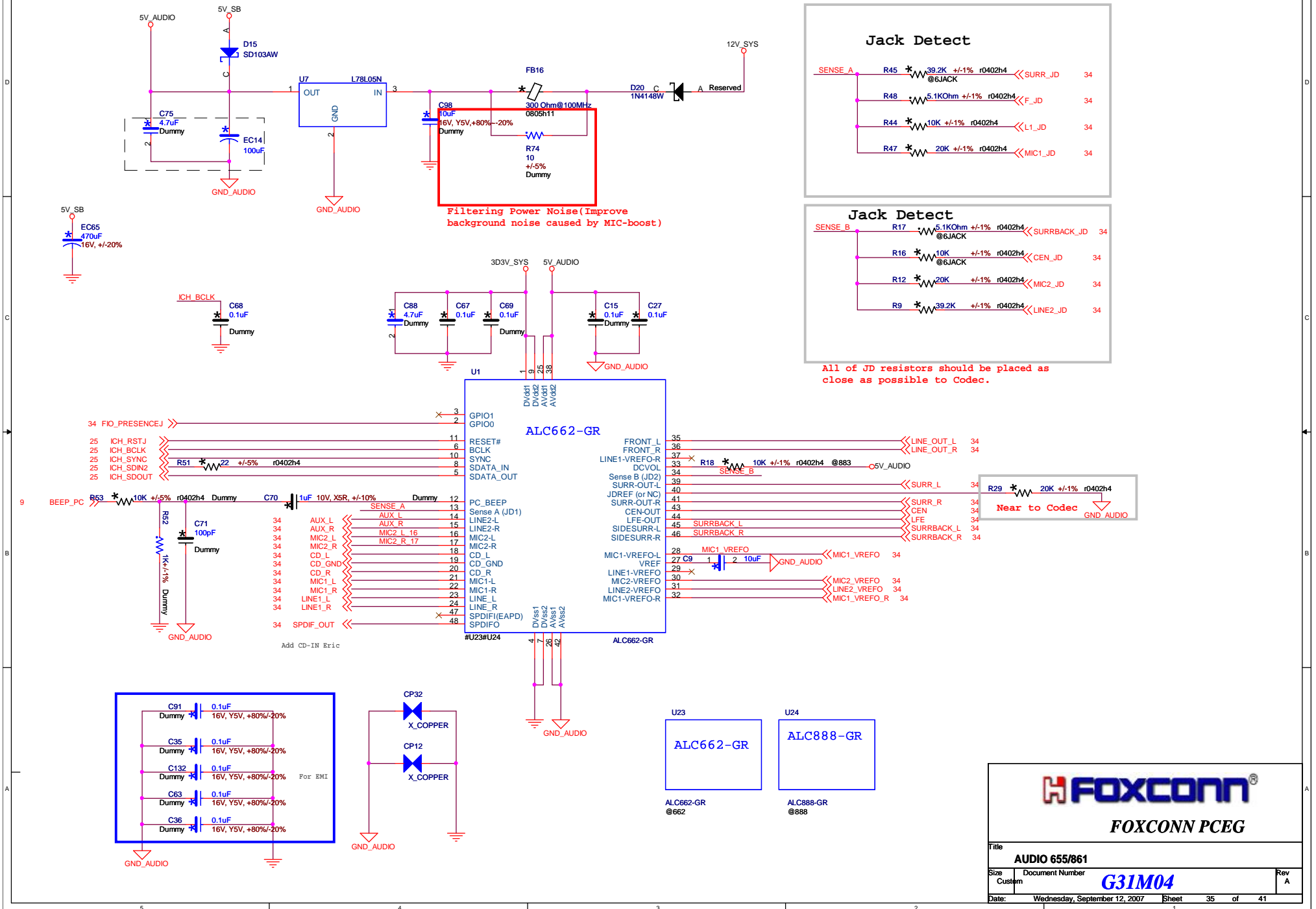


**FOXCONN PCEG**

Super IO ITE8712FAX

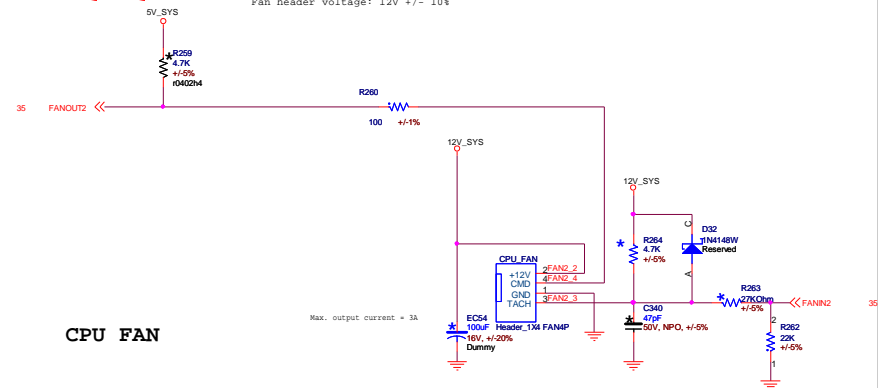
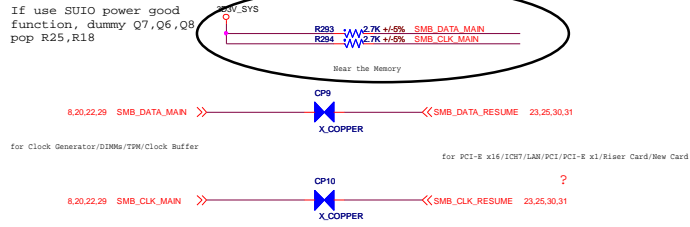
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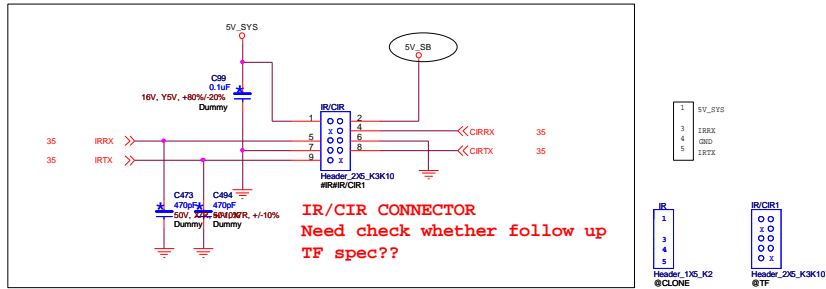


## SM Bus Bridge

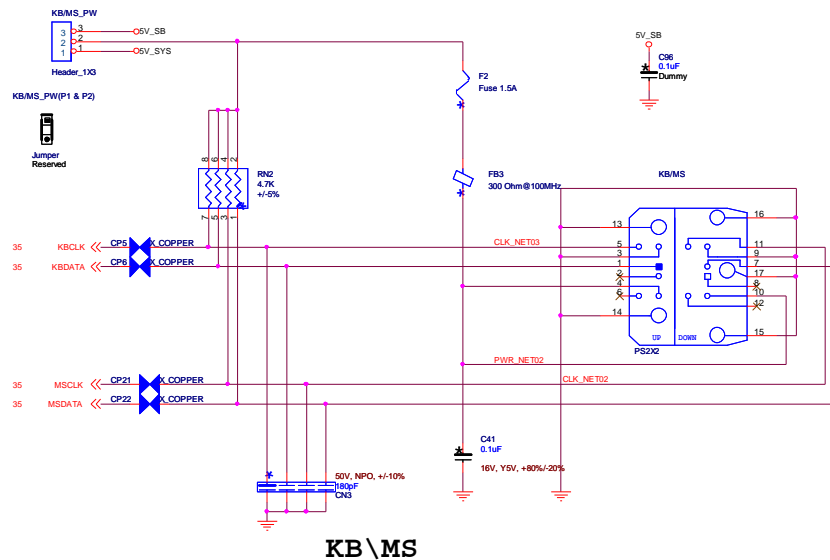
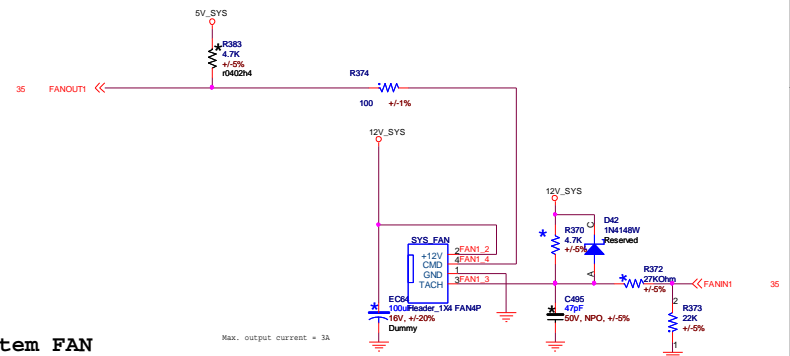
If use SUIO power good function, dummy Q7,Q6,Q8 pop R25,R18



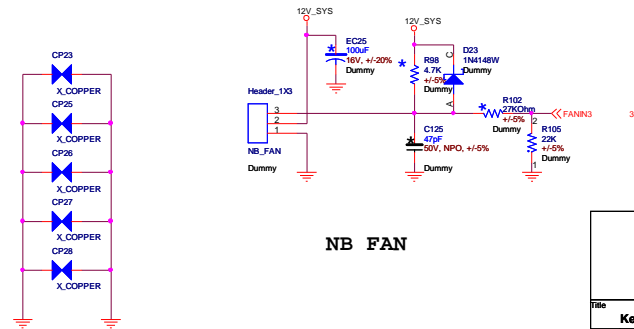
CPU FAN



System FAN

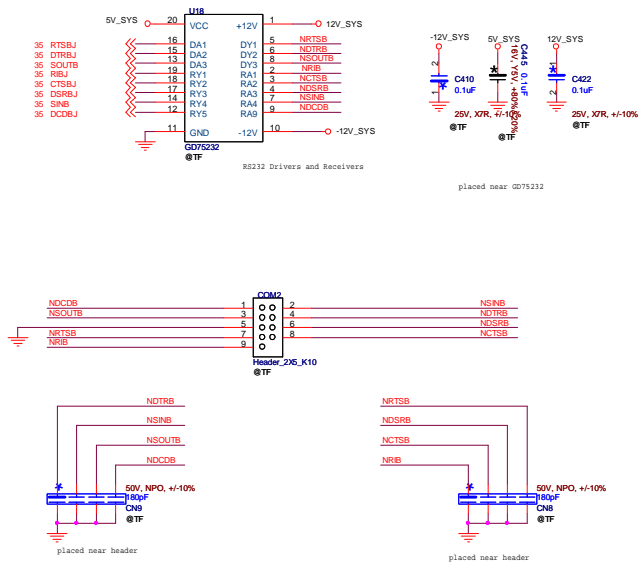


KB\MS

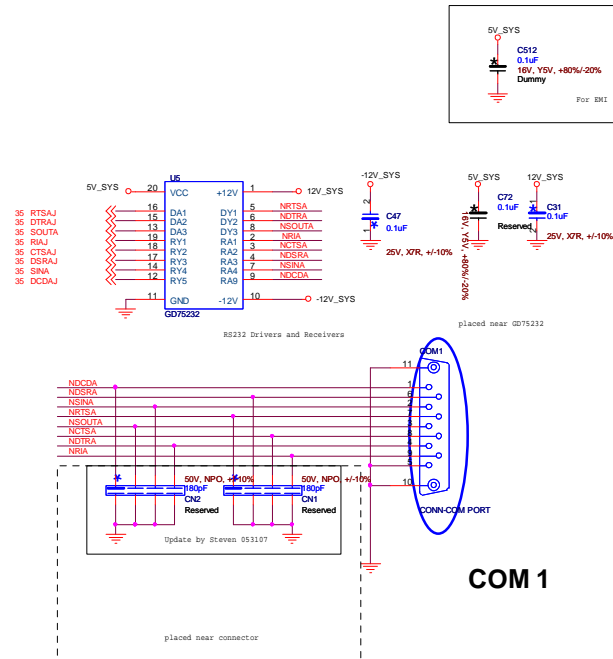


NB FAN

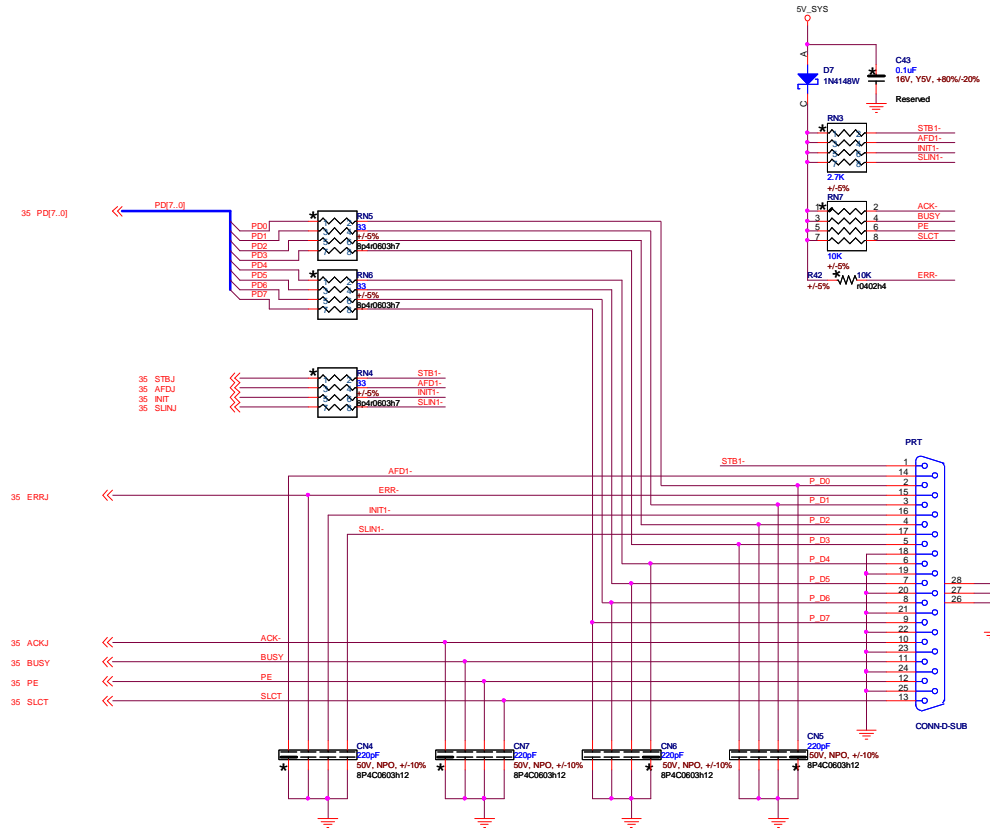
		<b>FOXCONN PCEG</b>	
		<b>Keyboard / Mouse / Fan</b>	
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COM 2 Header



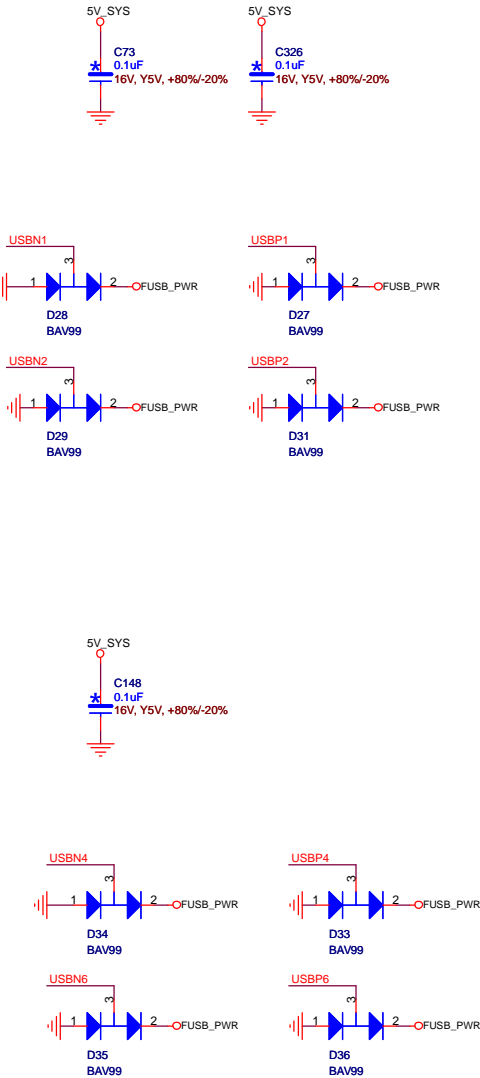
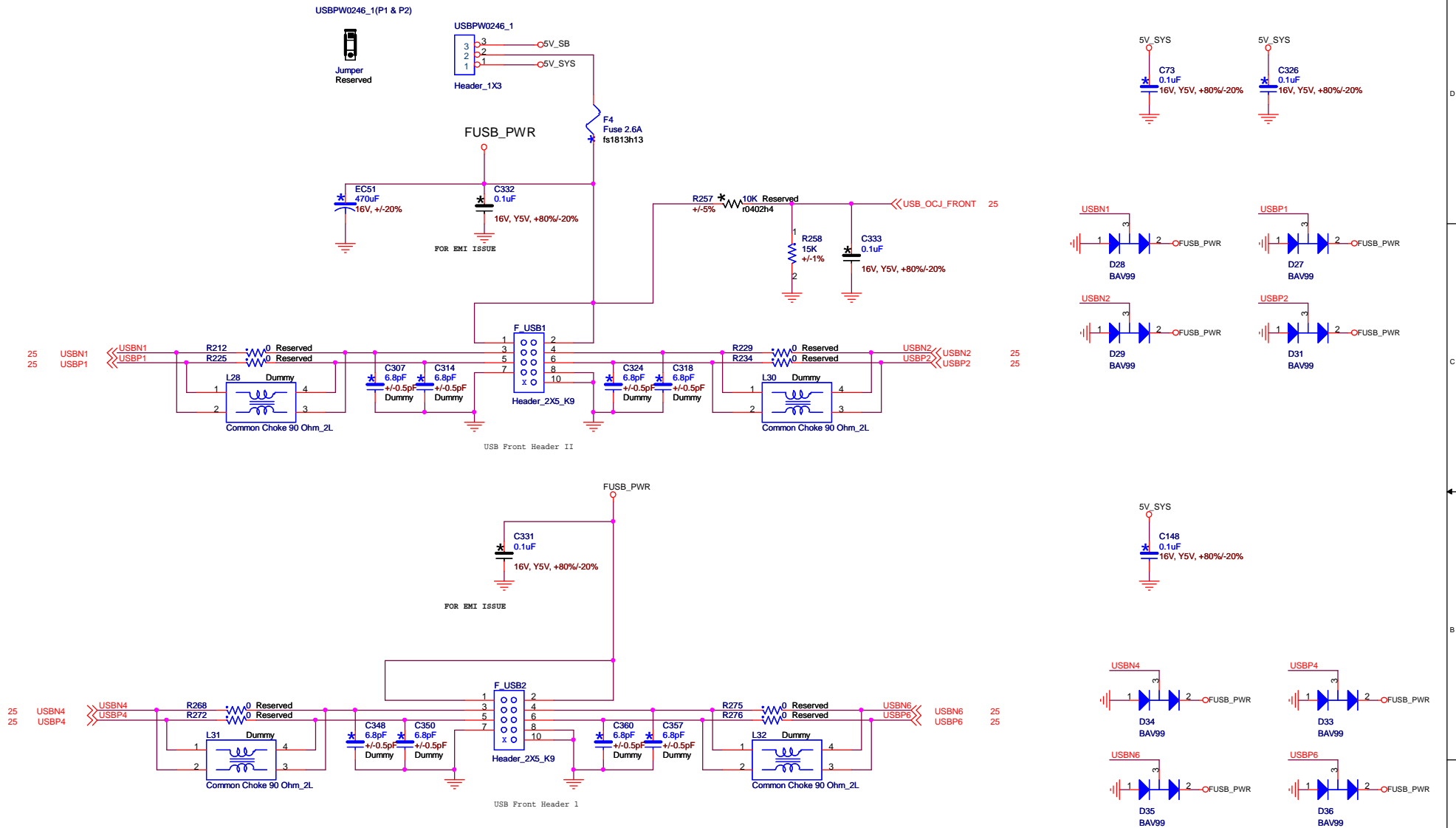
COM 1



PRT PORT

Ring

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**FOXCONN**

**FOXCONN PCEG**

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1. Change Lan RTL8111B colay RTL8101E to RTL8111C colay RTL8101E
  2. Change Audio ALC888 colay ALC883 to ALC662 colay ALC888
  3. Reserved Memory ratio schematic for over clock.
  4. Del R108,C139,Q22,Q20,R107 and then connect VRMPWGD directly for VRD11.
  5. Add R371,C501 for power button debounce circuit.
  6. Reserved U15,U17 for TF spec.
  7. Reserved TPM Header for TF spec.
  8. Reserved U3,U6 for TF spec.
  9. Add R8,R1,R5,R10,R6,R14,R87,R86,R85,R84,R78,R76,R73,R75,R41,R55 for Audio ESD
  10. Reserved CIR function for TF spec.
  11. Reserved NB FAN.
  12. Reserved C307,C314,C324,C318,C348,C350,C360,C357 for TF Front Panel
  13. Change R335 to 91ohm,R337 to 115ohm for Memory Power
  14. Remove R338 and stuff R332 for FAN half speed when Power on.
  15. Reserved R46 for realtek's suggestion
  16. Reserved U9,C144,C145 for VCCA\_DAC
  17. Add RT8111B SCH
  18. Del EC72,EC55,EC54,EC73 for placement issue
  19. Reserved R40,R25 For EMI
  21. Add C16,C17 For RTL8111B LAN Chip EMI
  22. Add FB22 For ITE suggestion
  23. Reserved C497 for Front Panel ESD
  24. Del Power V15SFR SCH
  25. Add R208,R220 for further CPU
  26. Reserved R321,R109,R320 for PCI RST
  27. Disconnect SLP\_S4 with CLK Gen
  28. Change C368,C371 from 18pF to 12pF
  29. Change F\_AUDIO Pin7 connect to Audio\_GND directly and connect Pin6,Pin10 to codec through the resistor.
- After Gerber Out:
30. Reserved C506
  31. Change R363 size from 0402 to 0603
  32. Change R111 to 33ohm 1%
  33. Add R400 100ohm 1%
  34. Dummy Q24 C146
  35. Reserved R94 In 8KS2H SKU
  36. Reserved R114,C147,R110,Q23,Q26
  37. Change R116,R118 to 10K 1%
  38. Change C160 to 1uF 0603
  39. Reserved Q39
  40. Del CP2
  41. Del EC29
  42. Reserved R356
  43. Change PCIE\_16x slot to 2EG48211-S7Y-4F
  44. Del EC65,EC66
  45. Add EC68
  46. Change L25,L38 to 630307400-176-G
  47. Reserved C451,C396,C375,C381,C430,C441,C355,C436,C447,C448,C397,C385,C446,C427,C405,C401,C395,C353,C390
  48. Del RN17
  49. Add R401,R402,R403 10K 5%
  50. Add JP1,JP2, JP1(P1&P2),JP2(P1&P2)
  51. Add R404 470ohm
  52. Add EC69
  53. Del EC46,EC47
  54. Change L26,L37 to APL1108P-2R5L
  55. Change C5,C6,C7 to 10pf
  56. Change L8,L9,L10 to GL1608082NJT
  57. Reserved C38,C65
  58. Change CP14 to L40 10uH
  59. Change L23 to 10uH
  60. Add C139,C513,C514 10uF
  61. Add EC65
  62. Del CP24
  63. Add R25 for EMC
  64. Add R409,R410,R411 for Audio codec ESD protection
  65. Change EC55 to 680uF
  66. Change L23 From 10uH Inductor to 10ohm Resistor

 <b>FOXCONN PCEG</b>	
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CHANGE LIST	
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